

An Optical Inspection System Development for Defects on Multi-surfaces of Chips

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Abstract. We proposed a new architecture with multiple pick and place heads to suck inspected chips and to be moved synchronously for acquiring the images of different surfaces on different chips at their corresponding acquisition stations. The computation loading of defect inspection for each chip also can be distributed because of sequential image acquisition. Considering the different computing loading of 6 surfaces of a chip, image acquisition for the front and back sides of chips is allocated at the first and second stations, and then 4 edge sides of chips. The modification and calibration of position and orientation for each opto-mechanical device will be simpler and easier when the characteristics of inspected chips changed. Thus system can accomplish the inspection for 6 surfaces of each chip and determine its quality in real-time before that chip is put onto target wafer. Developed inspection system has advantages and contributions of real-time inspection with high throughput during chip sorting process, and easily adjustment and calibration for all opto-mechanical devices to inspect different types of chips. The first phase of development was accomplished for an AOI system to inspect defects on 5 surfaces of chips. System has been integrated in customer's chip sorter for testing. The inspecting accuracy for chip backside is better than 95%.

1 Introduction

The thickness of 3DIC chips with circuit design both on front and back sides is thinner (<100 μm) than common IC chips due to application requirements. The cutting techniques then become the critical factor of cutting quality for these thin chips. But only few semiconductor companies with advantaged technologies own these cutting technologies. Chipping and glue could exist on chip surfaces of front, back and edge sides after cutting, and might impact chip quality and yield rate of manufacturing. In order to ensure the product quality, chips have to be inspected to feedback chips quality of production lines. The manufacturing processes then can be improved as well. Image acquisition and defect inspection for 6 surfaces of each chip shall be completed during chip sorting process according to customer's requirements. And chips need to be allocated on target wafer or tray in real-time. Then customers can reduce the wastes and costs of packaging the unqualified chips.

The main referenced patent related to multi-surface inspection of chips and applications is US 7283253 B2 [1]. A complicated opto-mechanical architecture, shown as Figure 1, for simultaneously acquiring images of 5 surfaces of chips is proposed in that patent. Its architecture seems rather convenient. But in fact, there're many constraints used for inspection. For example, different lighting sources are need to accommodate the

requirements of acquiring images for back and edge sides of chip and protruding features on images. Moreover, the system inspection performance will decrease substantially in operations because of the inspected chips have to be sunk into the structure of Opto-Mechanical Device (OMD).

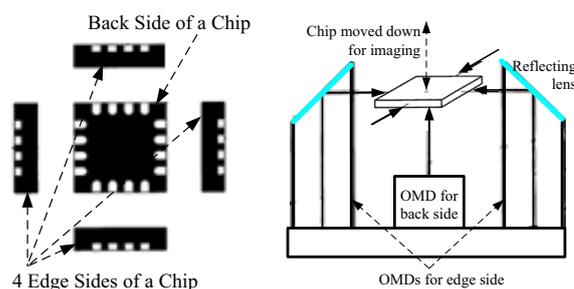


Figure 1. Diagram of an opto-mechanical device for images acquisition on 5 surfaces of chips in reference [1].

Owing to above limitations, most of patents and related applications were designed to extract its partial concepts and principles for developing new structures and applications. For instance, system consists of one OMD for acquiring image of chip back side and two OMDs for acquiring chip edge side. And there're 3 stations for multi-image acquisition of chips by using the multiple PP heads moved circularly. But inspected chips

still need to be sunk into the structure of OMDs, and the efficiency problem exists.

Here we proposed a new architecture consisted of multiple PP heads moved simultaneously to acquire images of corresponding chips at different positions for 6 surfaces of chips. The sequence of image acquisition for front and back sides of chips is disposed at 1st and 2nd stations considering that they need larger computation time. Then inspection system can complete the inspection for all surfaces and the quality determination of each chip before placed in GO/NG target wafer or tray. Therefore, the quality of chips can be accomplished in real-time during sorting process to achieve high efficiency of performance. The qualified chips then can be rearranged on target wafer for follow-up packaging and quality tracing.

2 System architecture and design

AOI system for detect defects on 6 surfaces of chip consists of 6 OMDs and their corresponding software modules, and infrastructure based on industrial personal computer (IPC) platform for system integration and operations. Developed AOI system was designed to inspect chip defects during sorting process with high inspecting performance.

The operations scenario and external interfaces have to be described as clearly as possible. Thus we can correctly define the system architecture, requirement specifications, function blocks and internal interfaces completely. The operation scenario and architecture of AOI system for 6 surfaces of chips can be schematically shown in Figure 2.

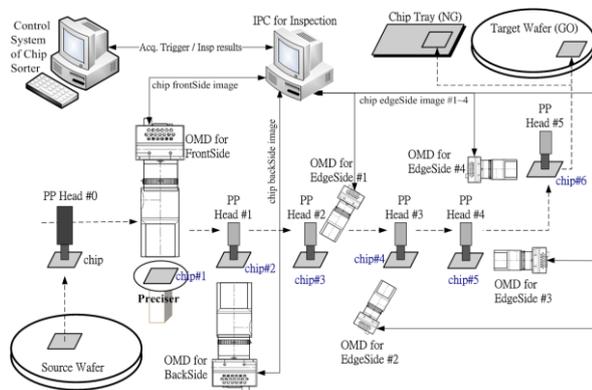


Figure 2. Operations scenario and architecture of AOI system for chips.

Control system of packaging machine sends the trigger signals of image acquisition for each OMD according to inspecting procedures. Each OMD immediately acquires and stores image for different surfaces of 6 chips simultaneously after receiving the trigger signal. Then 6 modules of inspection software conduct the image processing and defect inspection in real-time based on acquired raw images. A chip is located at different stations sequentially to acquire all images of its 6 surfaces. After finishing the image acquisition and defect inspection for the chip located at 6th station, the quality of the chip therefore can be determined. The

inspection results for each chip are transmitted to control system. Then the qualified chip is rearranged on target wafer and unqualified chip will be put in tray of NG.

2.1 System requirement specifications and analysis

- (1) Inspecting targets for 6 surfaces of chips
 - Front and back sides of chip: Defect size of glue or contaminant on surface, and chippings at the rim of chip is greater than the inspecting criteria.
 - Edge side of chip: Defect size of glue or chippings is greater than the inspecting criteria for 4 edge sides.
- (2) Specifications for opto-mechanical devices
 - OMD for image of chip front side: Spatial resolution for each pixel on image shall be better than $1.57 \mu\text{m}$. Chip size of no greater than $7.2 \times 6.8 \text{ mm}$ can be inspected.
 - OMD for image of chip back side: Spatial resolution for each pixel on image shall be better than $3 \mu\text{m}$. Chip size of no greater than $7.2 \times 7.2 \text{ mm}$ can be inspected.
 - OMD for image of edge sides: Spatial resolution for each pixel on image shall be better than $3.45 \mu\text{m}$. Chip size of no greater than $7.2 \times 5.6 \text{ mm}$ can be inspected.
- (3) Specifications for defect inspecting criteria
 - Defects on front side: Defect size of greater than $8 \times 8 \mu\text{m}$ for glue or contaminant shall be detected. Both the depth of chippings from chip boundaries and their corresponding width of greater than $21 \mu\text{m}$ shall be inspected.
 - Defects on back side: Defect size of greater than $10 \times 10 \mu\text{m}$ for glue or contaminant shall be detected. Both the depth of chippings from chip boundaries and their corresponding width of greater than $21 \mu\text{m}$ shall be inspected.
 - Defects on edge side: Defect size of greater than $10 \times 10 \mu\text{m}$ shall be detected for glue or chipping.
- (4) Requirement specifications for inspection accuracy
 - Error rate for inspecting front side of chip $< 5\%$.
 - Error rate for inspecting back side of chip $< 10\%$.
 - Error rate for inspecting edge side of chip $< 5\%$.

The AOI system for 6 surfaces of chip comprises 6 OMDs for front side, back side, 4 edge sides of chips, and their corresponding inspection software (S/W) modules, and an IPC platform. Each OMD includes the functions of illumination, image acquisition and storage. Each inspection software includes the modules of image preprocessing, chip image extraction and defect inspection. The system integration and tests for OMDs, software modules and packaging machine shall be accomplished to simultaneously fulfill all functions and performance of sorting and inspection for chips.

2.2 Design for opto-mechanical device

COTS products are adopted for all lenses and cameras of OMDs considering their quality, stable sources, and

flexibility of update for critical modules. Key features of COTS critical modules for 3 types of OMDs are briefly described as below:

- (1) OMD features for chip front side
 - Camera: Size of CCD sensor is 5.5μm. Image resolution is 29M with data interface of camera link (CL). EureSys GrabLink Full card [2] is selected.
 - Lenses: Magnification is 3.5. Resolution and DOF are about 1.2μm and 13μm respectively. Both of ring and coaxial lighting modules are designed.
- (2) OMD features for chip back side
 - Camera: Size of CCD sensor is 4.5μm. Image resolution is 25M.
 - Lenses: Magnification is 0.5~2.0. Resolution and DOF are about 3μm and 500μm respectively [3]. Both of ring and coaxial lighting modules are included.
- (3) OMD features for chip edge sides
 - Camera: Size of CCD sensor is 3.45μm, and image resolution is 5M with GigE data interface.

2.3 System functional block and interfaces

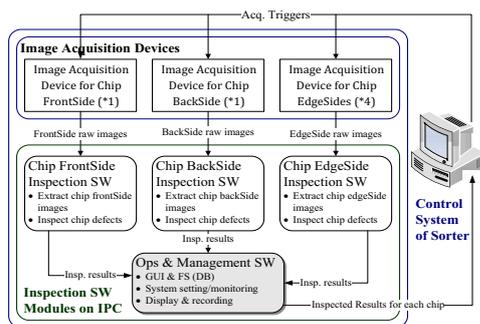


Figure 3. System Functional Block Diagram and Interfaces.

Developed inspection system for multi-surfaces of chip consists of following OMDs and software modules:

- (1) OMD and S/W module for chip front side: The spatial resolution of acquired image is 1.57μm/pixel and FOV is about 10.32 x 6.88 mm. Inspection S/W module real-time read images of provided by OMD via CL interface. Image processing by using methods of frequency domain analysis for image registration and template-based matching for defect detection are applied. Defective chips will be designated and reported for quality evaluation and classification if the size of defects is greater than criteria.
- (2) OMD and S/W module for chip back side: Ring illuminating modules is used for acquiring the dark field image of chip backside. But coaxial lighting module is also designed for inspecting few defects of hard to be detected. The spatial resolution of image is 3 μm/pixel and FOV is about 15 x 15 mm. Chip backside image of dark field is applied for inspection S/W module. Image enhancement is applied to stand out the defects on backside image [4].
- (3) OMD and S/W module for chip edge side: The spatial resolution of image is 3.45 μm/pixel and FOV is

about 7.3 x 6.1 mm. S/W module for inspecting defects of chip edge side, including glue and chipping.

S/W module for operations and management can provide the functions of system setting and monitoring, and graphic user interfaces (GUI). Inspection system was integrated with chip sorter. Qualified chips will be rearranged on target wafer, and the defective chips will be allocated in NG tray after chip sorter receives the inspection results of each chip. Figure 3 shows the functional block diagram of developed system.

3 Inspection methods for 6 surfaces of chips

3.1 Defect inspection for front side of chips

Inspection methods and flowchart for chip front side are depicted in Figure 4. Images are processed by registration [5, 6], including rotation, scale and position, based on the template chip image. Defects can consequently be detected by using background filtering and pattern matching [7, 8]. The inspection algorithm for front side of chip now is still being improved to achieve higher accuracy and performance of inspection.

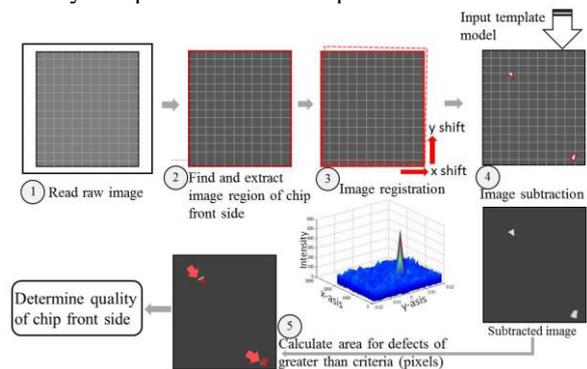


Figure 4. Inspection methods and flowchart for chip front side.

We can consider the defect inspection on images as the problem of background subtraction. The chip images with regular type or profile are regarded as “background”. The region with intensity difference between inspected image and background image are the “foreground”. We can therefore designate and determine these foregrounds as defects with features or size of greater than criteria [8]. The background model used as matching template here is generated by Gaussian Mixture Model (GMM) [9]. There're few variation of pixel intensity for designated point on acquired images due to the small change of illumination, the machine vibration and so on.

The update of background model includes the derivation of Gaussian model for template update. The pixels intensity of images under different time, , , ..., , can be described by Gaussian distribution respectively. Hence we have following equation:

$$P(I_t) = \sum_{k=1}^K \omega_{t-1,k} N(I_t; \mu_{t-1,k}; \sigma_{t-1,k}^2) \quad (1)$$

where σ is Gaussian distribution function, μ , and σ are mean value, variance and weighting factor respectively.

3.2 Defect inspection for back side of chips

The methods and flowchart for chip backside inspection are depicted in Figure 5. After the image of chip area is segmented, the dark field image of chip backside will be pre-processed by image enhancement to make defects more clearly on chip image. We then can inverse the gray-level of image to derive an inverted image. Defects of glue, contaminant and boundary chipping can be derived by blob/contour finding. The size of defects of greater than criteria will be designated and reported for quality check.

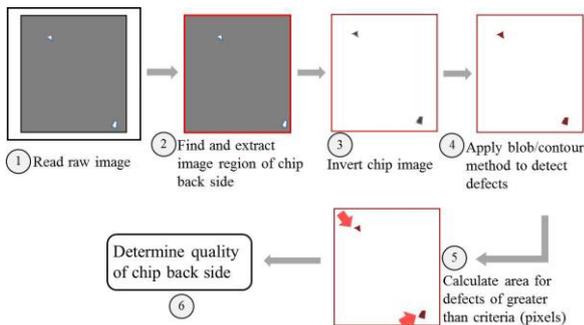


Figure 5. Inspection methods and flowchart for chip backside.

3.3 Defect inspection for edge sides of chips

Figure 6 is the flowchart and methods of defect inspection for chip edge sides. We designate the region of edge side of chip, and then extract the chip area [10, 11]. Thus the defects of glue and boundary chipping can be derived by using methods of blob/contour finding. And the defects of greater than criteria are designated and reported.

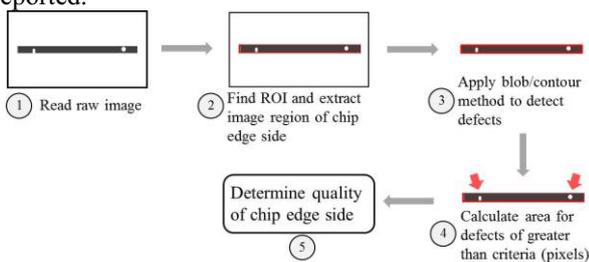


Figure 6. Inspection methods and flowchart for chip edge side.

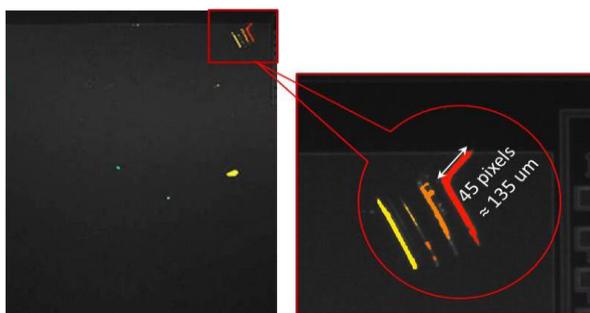


Figure 7. Defects size on chip back side detected by developed AOI system.

4 Experiments and discussion

The prototypical inspection system for 5 surfaces of chip has been implemented and integrated with chip sorters. The defects on chip backside are inspected by dark field image as shown in Figure 7. Defect size of inspected by developed AOI system is also depicted in Figure 7. Measured result for the same defect by microscopy is shown in Figure 8. The size error of defect on chip backside is within 1 pixel (3um) compared to the measured result by using microscopy.

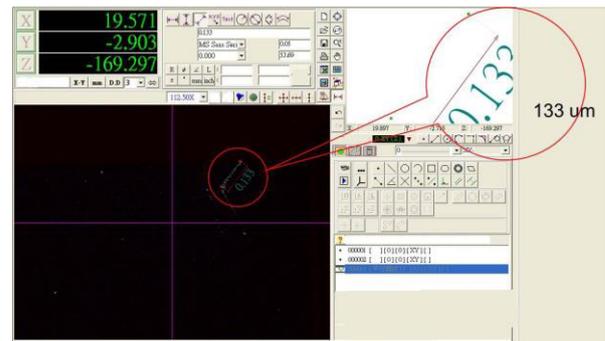


Figure 8. Defects size on back side of chip measured by microscopy.

Based on the preliminary test results of inspection, the accuracy of inspection for developed system is better than 95% for backside of chips. Now we continuously improve the image quality and inspection methods to try raising the performance and accuracy of inspection.

The defects size for an edge side of a chip, detected by developed system and measured by microscopy, are shown in Figure 9 and 10 respectively. The inspection error is within 1 pixel (3.45um) as well. But defects of glue and chipping can't be discriminated because of their reflective features on image are very similar. Cutting scars on images of chip edge sides is another problem to decrease the inspecting accuracy.

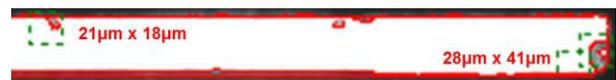


Figure 9. Defects size on chip edge side inspected by developed AOI system.

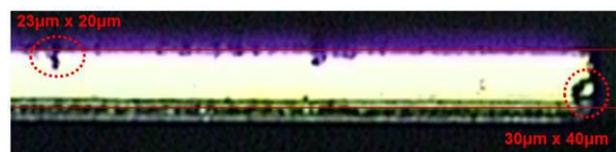


Figure 10. Defects size on chip edge side measured by microscopy.

Figure 11 is the inspection result for front side of a chip by our developed system. Defects on front side can be inspected successfully, but the inspection accuracy needs to be verified by using more images in the near future. And we still try to improve the inspecting algorithms for chip front side continuously for the moment.

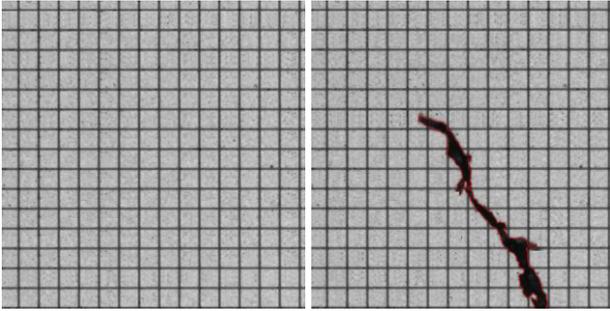


Figure 11. Inspection result for front side of a chip (left: good chip, right: inspected chip with defects)

5 Conclusion

An AOI system with new architecture of imaging devices for defects on multi-surfaces of chips was developed and presented in this work. System comprises 6 OMDs to acquire raw images for their corresponding surfaces on different chips, inspection S/W modules, and industrial PC platform. The first phase of developing an AOI system for defects on 5 surfaces of chips was accomplished. System has been integrated in customer's chip sorter for testing. The inspecting accuracy for chip backside is better than 95%. Defects with flat feature which is peeled off chip boundary can't be detected constantly. Therefore, bright-field images need to be applied to improve the inspection accuracy in our future work. Another challenge is the cutting scars on chip edge side that will interfere with inspection accuracy, and have to be handled continuously.

Comparing to other similar AOI system, developed system here with multiple PP heads to suck different chips for simultaneously acquiring images on 6 surfaces of chips has better system throughput and is easily adjusted for different types of chips. Chips can be inspected in real-time during sorting process for quality assurance to improve the production efficiency.

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