

Research on current sharing of paralleled IGBTs in different DC breaker circuit topologies

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Abstract. IGBT modules used in series and parallel to satisfy the requirement in high-power DC circuit breakers are often prone to large-current destruction due to current unbalance between paralleled IGBTs. It is of great importance to identify the current unbalance causes and to find a method optimizing the current sharing of paralleled IGBTs. In this paper the current-sharing influencing factors are discussed and verified by simulation. Two possible circuit topologies used in DC circuit breakers are proposed and simulated to see their performance in current sharing. The results show that one of them can provide us with a simple and effective method to achieve good current balancing in the DC circuit breaker application.

1 Introduction

DC breakers are increasingly being used in many power electronic applications such as Flexible AC transmission systems (FACTS) and high-voltage direct current (HVDC) transmission systems [1]. Currently, these applications are often operated at progressively higher power levels and in order to fulfil this demand, power semiconductor devices used in these applications need to reach a high power level. Among all the semiconductor devices used in such circumstances the insulated-gate bipolar transistor (IGBT) is a major representative with advantages like easy driving, low power dissipation and snubberless operation [2][3]. During the past few decades, developments in semiconductor technology have led to fast advance in high-power IGBTs [4]-[11].

Although The blocking voltages of these IGBTs rise up to 6.5 kV and current ratings are steadily increasing [12][13], they cannot fully meet the high power requirement and are often connected in parallel due to their limited power capacity[14][15]. When the power and voltage ratings are within the limit, it is also advantageous to use several IGBTs with lower ratings in series and parallel to cut the cost. But unfortunately the current (voltage) imbalance between parallel (series)-connected IGBTs can lead to imbalance temperature and losses, as well as over voltage or current destruction, so attention should be paid during the IGBT module design [3]. The factors causing the imbalance are similar for both the voltage and the current sharing, and here we mainly focus on the later. The current balance influencing factors falls into 3 categories: the device characteristics, the gate-drive circuit and the main circuit design [2]-[11]. Many efforts have been made in order to achieve equal current sharing in the parallel-connected IGBT modules

[16]-[19]. However, these methods are rather wasting or complicated.

In this paper we discuss the current balancing performances of 2 alternative topologies to see if any of them can provide us with a simple and effective method to achieve good current balancing in the DC circuit breaker application. In the first part we review the electrical characteristics of the IGBTs and discuss the factors influencing the turn-on, turn-off, and the steady state. In the second part we illustrate the effect of each major influencing factor with the Saber software. Then we provide the 2 possible circuit topologies used in a dc circuit breaker and analyze their performances.

2 Electrical characteristics of IGBT and influencing factors

The IGBT symbol and the equivalent circuit is shown in Fig. 1. The device can be seen as a voltage-controlled current source and an equivalent resistance r , together with parasitic capacitances, inductances and resistances [20]. The IGBT switching process can be divided into the steady state and the transient. The main factor influencing the steady state is the equivalent resistance, and this is related to the saturation voltage and the collector current. For the transient, the key factor is the gate current and this is decided by the gate-drive voltage, the internal gate resistor r_g , the external gate resistor R_g , and the capacitances C_{GE} and C_{CG} . To explain this, the turn on and turn off behavior of the device should be first introduced.

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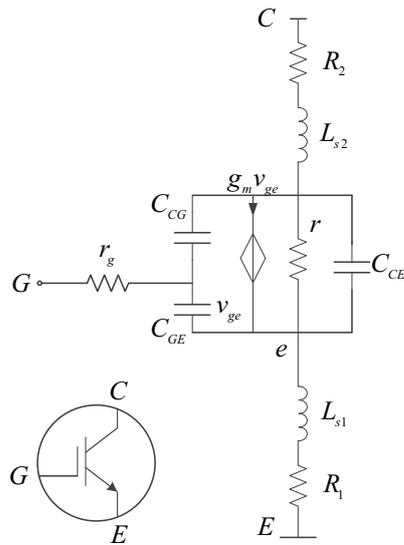


Figure 1. Equivalent circuit of an IGBT.

As can be seen Fig. 2, the processes of turning on and off can be each divided into 3 phases. During the turn-on process the gate voltage starts rising right after the driving voltage is given, and when it reaches the threshold V_{th} the collector current begins to rise. When the current stops rising the gate voltage experience a short break at V_M , and during this break the collector-emitter voltage starts to fall until the gate voltage begin to rise again. The turn-off process is the reverse of the turn-on process.

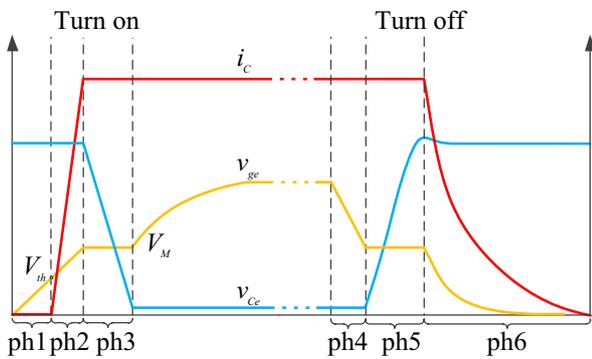


Figure 2. Turn-on and turn-off waveforms of an IGBT.

To get a better understanding of the waveforms and to find out the influential factors of the waveform features, it is necessary to see what happens inside the IGBT during the turn-on and turn-off process. The equivalent gate circuit of an IGBT is illustrated in Fig. 3.

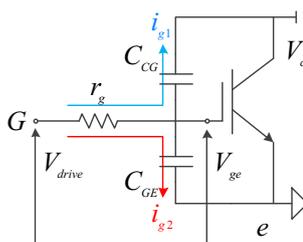


Figure 3. The equivalent gate circuit of an IGBT.

The increase of the gate voltage indicates that the gate current is charging the capacitor C_{GE} and when the voltage across the capacitor is higher than the threshold V_{th} the collector current starts to rise. Later when voltage of C_{GE} comes to the Miller plateau the current stops rising. During the Miller plateau the gate current charges C_{CG} and when it's fully charged the gate current goes back to C_{GE} again. So this process indicate that the charging speed is determined by the gate current magnitude which further depends on the gate-drive voltage, r_g , and R_g , while the Miller plateau is related to C_{GE} and C_{CG} . The turn-off process is the reverse of that of the turn on.

According to Fig. 3 the following relationships can be obtained.

$$i_g = \frac{V_{drive} - V_{ge}}{r_g} \quad (1)$$

$$i_g = i_{g1} + i_{g2} \quad (2)$$

$$i_{g2} = C_{GE} \frac{dV_{ge}}{dt} \quad (3)$$

$$i_{g1} = C_{CG} \frac{d(V_c - V_{ge})}{dt} \quad (4)$$

If we assume that V_c is fixed, which is true in most cases, the time of each phases in the turn-on process in Fig. 2 can be obtained as

$$t_{ph1} = (R_g + r_g)(C_{CG} + C_{GE}) \ln \left[1 / \left(1 - \frac{V_{th}}{V_{GD}} \right) \right] \quad (5)$$

$$t_{ph2} = (R_g + r_g)(C_{CG} + C_{GE}) \ln \left[1 / \left(1 - \frac{V_M}{V_{GD}} \right) \right] - t_{ph1} \quad (6)$$

$$t_{ph3} = \frac{(V_c - V_F)(R_g + r_g)C_{CG}}{V_{GD} - V_M} \quad (7)$$

where V_M is the gate Miller plateau voltage, V_{GD} refers to the applied gate-drive voltage, R_g is the external gate resistance, and V_F means the on-state voltage drop. From the analysis above we can figure out that the influential factors of the transient are the threshold voltage, capacitances, gate resistances, stray impedances in the branches and the time delay. For the steady state, the influential factor is the equivalent resistances in each IGBT branch.

3 Simulation verification of the effect of influencing factors

To further study the effect of the influential factors mentioned above one by one, the software Saber is used for the simplicity in separating the effect of each factor. Two IGBT modules are connected in parallel with different gate drives, as shown in Fig. 4.

The simulation result is shown in Fig. 5. The IGBT on state resistance and the line resistances, as well as the external and internal gate resistances are similar factors so only one of the two in each pair is shown. As can be seen from the figure, the gate-emitter capacitance, the time delay and the gate resistance have important impact on the current sharing of two paralleled IGBTs. The line resistance affect the current sharing greatly in steady state.

The less important factor is the threshold voltage and the least is the line stray inductances. The simulation results coherent with the calculated results.

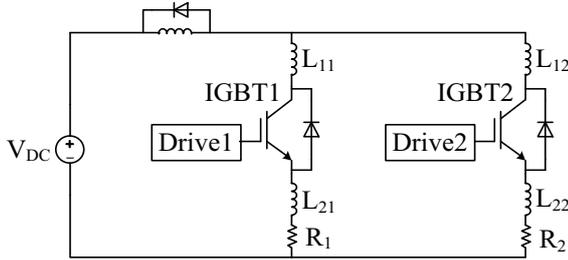
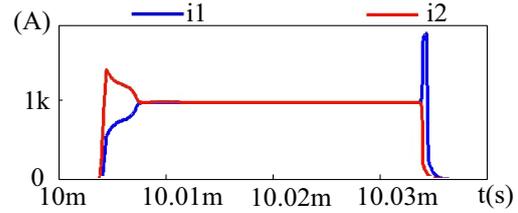
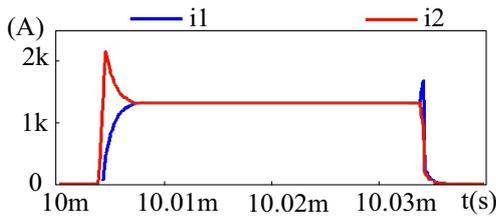


Figure 4. The simulation circuit.

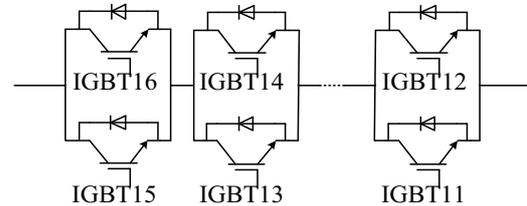


(f) $R_{g1}=130\%R_{g2}$.

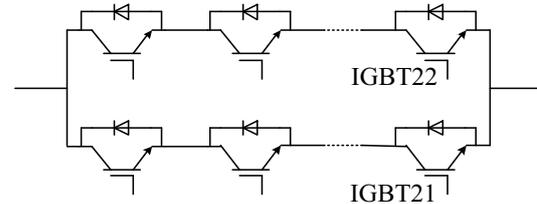
Figure 5. The simulation result.

4 Two alternative topologies and their performance analysis

In the DC circuit breaker application, two types of series and parallel connection of the IGBTs are possible, as illustrated in Fig. 6.



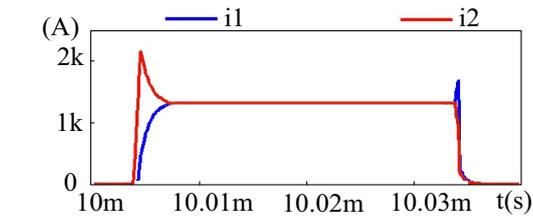
(a) Topology 1.



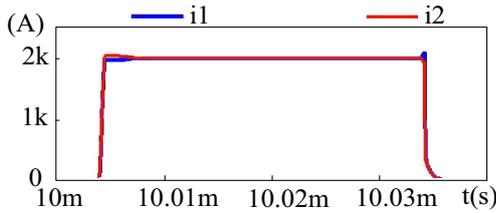
(b) Topology 2.

Figure 6. The alternative topologies.

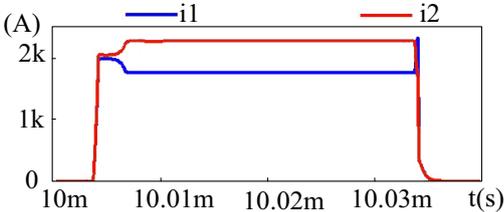
The two topologies are set under simulation to see their performances. Three pairs of IGBTs are presented in the simulation topology and parameters of IGBT11 and IGBT21 are changed in each case. The currents in the related branches, i.e. i_{11} , i_{12} , i_{21} , i_{22} , are detected and the results are shown in Fig. 7. It is necessary to note that topology 1 can be seen as three identical sub-systems each formed by two paralleled IGBTs (e.g. IGBT11 and IGBT12), and the characteristics of every sub-system are the same as described in part 3. Consequently, the current is re-shared in each sub-system in topology 1. As can be seen from Fig. 7, the unbalance degree of topology 2 is much smaller than that of topology 1, and when the number of IGBTs increases, the unbalance degree of currents in parallel further decreases. This is because in topology 1 all the IGBTs other than IGBT11 have the same parameters in purpose of comparing with topology 2, so the current unbalance is just subjected to the aimed sub-system (i.e. IGBT11 and IGBT12) while in topology 2 the unbalance is shared by the other IGBTs. So a conclusion can be drawn that when certain degree of unbalance in current is allowed, it is better to use the



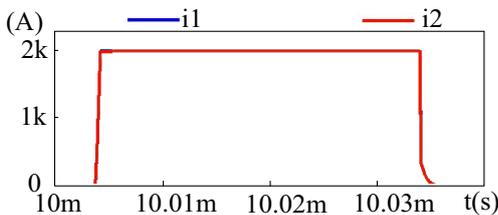
(a) $C_{ge1}=130\%C_{ge2}$.



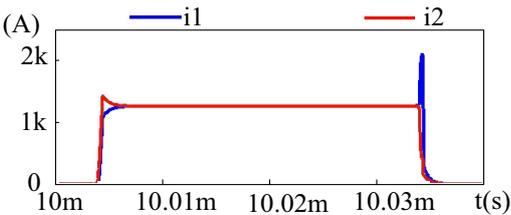
(b) $V_{th1}=130\%V_{th2}$.



(c) $R_1=130\%R_2$.



(d) $L_{11}=130\%L_{12}$.



(e) IGBT1 delay 100ns.

second topology and choose IGBTs of smaller rated current and voltage to increase the number of devices.

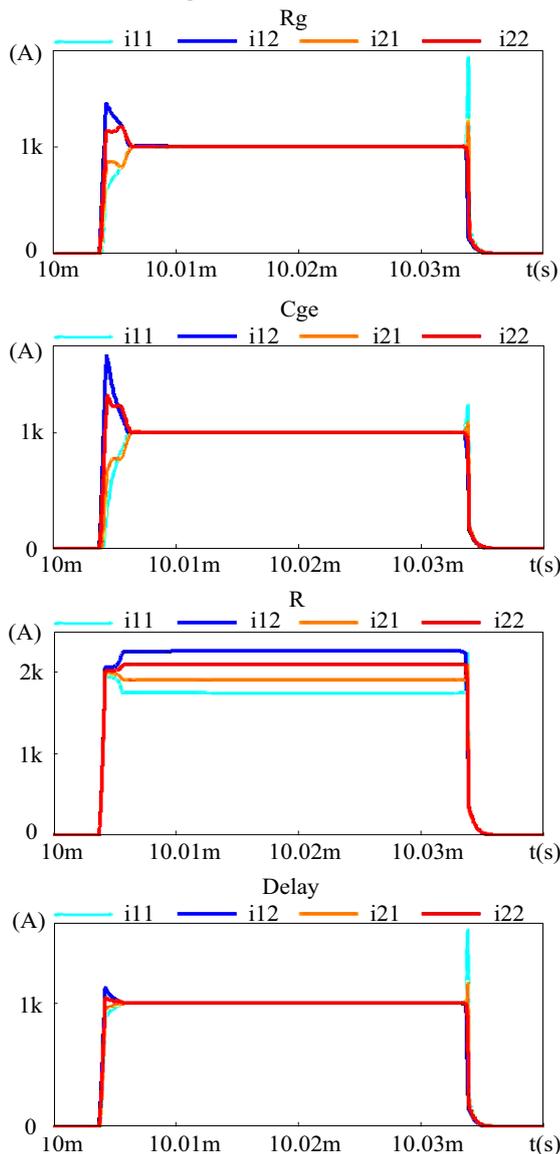


Figure 7. The alternative connecting topologies.

5 Conclusion

In this paper, the electrical characteristics of the IGBTs are reviewed and the current-sharing influencing factors of parallel-connected IGBTs are discussed. The effect of each major influencing factor is illustrated with the help of software Saber. Two possible circuit topologies used in a DC circuit breaker are proposed and simulated to see their current balancing performances in order to find out if any of them can provide us with a simple and effective method to achieve good current balancing in the DC circuit breaker application. It is shown that one of the alternative topologies has certain self-balancing effect and performs better under the same conditions. The result can help with better design of the DC circuit breakers especially in high-power applications when the devices have to be connected in series and parallel. Future work will involve the experimental verification of the performance as well as the reliability analysis.

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