Design of EMCCD Driving System for Underwater Low-Light Camera

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Abstract. For the core of underwater low-light camera, i.e. EMCCD, the whole solution of driving system is presented in this paper. The timing signals which meet the driving requirements of EMCCD are produced from FPGA. The high-speed integrated driver chips convert the timing signals into general power driving signals with the amplitude under 12V; a Class A push-pull amplifier circuit built in discrete components transforms the timing signals into high-voltage multiplying signals. Besides, the impedance matching for the circuit optimizes the driving system. The experimental results indicate that the driving system generates the high-voltage multiplying signals, with their high level adjusted from 30V to 48V and frequency raised up to 10MHz. The whole driving system satisfies the requirements of EMCCD, and has the capability to ensure the normal operation of EMCCD.

1 Introduction

Determining the damage degree of shipwrecks quickly and precisely is the precondition for drawing up and implementing the scheme of underwater salvage. At present, the exploration of the damage degree of shipwrecks is usually realized by recording images with general high-resolution camera. However, secondary light source need to be utilized in the low-light underwater conditions. In this case, the performance of general high-resolution cameras reduces greatly because of the backscattering of water-body, so that high-quality images cannot be obtained. For the purpose of overcoming the problem, the underwater low-light camera with the ability to detect weak light emerged at the right moment.

With its favourable characteristics such as high quantum efficiency, high sensitivity, high readout rate, ultra-low readout noise and adjustable gain [1], EMCCD (Electron-Multiplying Charge Coupled Device) can take high-definition images in the deep sea with hardly any illumination. Therefore, it is utilized as the core of the underwater low-light camera. In the whole design of the driving system, it is difficult to generate the high-voltage multiplying signal, which is the most important part of the application of EMCCD [2]. In addition, the scheme design for the driving system and the establishment of the system which makes the EMCCD work well based on the design lay the foundation for the overall system design of the underwater low-light camera.

2 CCD97 overview

Produced by E2V in the United Kingdom, CCD97 is a type of frame transfer area EMCCD [3]. CCD97 utilizes the technology of gaining on-chip. While the readout frequency is 11MHz, the output noise can be inferior to the level of an electron [4]. As a consequence, CCD97 is chosen as the core of underwater low-light camera.

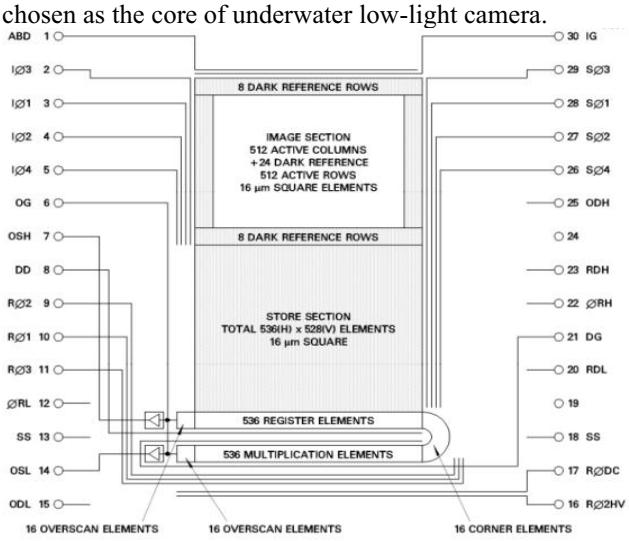

Figure 1. Structure chart of CCD97.

As shown in Figure 1, the active image area of CCD97 is 8.192×8.192 mm^2, and the image pixel size is 16×16um^2. The number of image section pixels is 528(H) ×536(V). In practical application, there are 8 dark pixels at the beginning and end of each line, and 12 at the beginning and end of each row [5]. These dark pixels covered completely by aluminium shells without outside light source is used as the reference of dark noise. As a result, the number of active pixels in the image section is 512(H) ×512(V). The corresponding store section has 528(H) ×536(V) elements to store the charge produced in the image section. When reading out the image signals

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from OSL (multiplication output channel), the charge will go through 536 register elements and 16 corner elements in the lower right corner, then the charge enter into 536 multiplication elements. Before entering the sense amplifier, the charge is multiplied in order to reduce the influence caused by the sense amplifier [6].

To give full play to the performance of CCD97, the low-noise driving circuits and bias circuits are necessary [7]. Except for RΦ2HV, the amplitudes of other driving signals are under 12V. RΦ2HV is the high-voltage multiplication signal, with an amplitude up to 50V which is adjustable. The frequency of driving signals that matches the output signal is 10MHz. Nevertheless, the phases of signals should be adjustable, and the drive capability neither too strong to cause a large overshoot voltage nor too weak to influence the operation of CCD97. Consequently, the design of driving system should consider amplitude, frequency, phase and driving capability [8].

3 Overall structure of underwater low-light camera

As presented in Figure 2, the overall structure of underwater low-light camera mainly contains three parts: EMCCD module, AFE module and FPGA module. FPGA module, as the control centre of the whole system, receives the commands from the computer through the RS422 interface and generates the driving signals utilized as the input of the peripheral driving circuitry of CCD97 on the EMCCD module. Through the peripheral driving circuitry, the driving signals are converted into the power driving signals that meet the requirements of CCD97, which then converts the light signals into analogue signals. Through the coaxial cable, analogue signals enter into the AFE module with the functions such as correlated couple sample, black level clamp, programmable gain amplifier and analog-to-digital converter. The digital signals converted by the AFE module are processed by the FPGA module and finally transmitted to the computer through LVDS driving module.

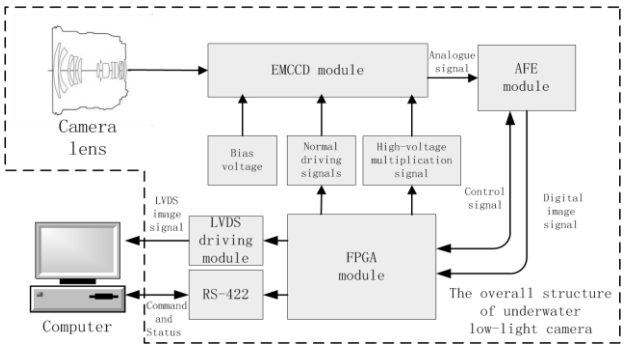

Figure 2. Overall structure of underwater low-light camera

4 Design of EMCCD driving system

The design of EMCCD driving system involves the hardware driving circuit of EMCCD and production of timing signals by FPGA.

4.1 Hardware part

For the normal operation of CCD97, 14 driving signals are necessary. According to the requirement of driving CCD97, the driving signals are divided into the general driving signals and the high-voltage multiplication driving signals. The former takes on the characteristics of low amplitude, high frequency and large load, in which case, the high-speed integrated driving chip meets the requirements of design. For the latter——RΦ2HV, the amplitude reaches up to 50V, which cannot be achieved by the high-speed integrated driving chip. Given this, the driving circuit is made up of discrete components. The amplitudes of driving signals are shown in Table 1.

Table 1. Amplitudes of driving signals.

Name		PULSE AMPLITUDE（V）		
		MIN	TYPICAL	MAX
IΦ1,2,3,4	HIGH	+5	+7	+9
	LOW	-6	+5	-4
SΦ1,2,3,4	HIGH	+5	+7	+9
	LOW	-6	+5	-4
RΦ1,2,3	HIGH	+8	+12	+13
	LOW	-	0	-
ΦRL, ΦRH	HIGH	0	+10	-
	LOW	0	0	-
RΦ2HV	HIGH	+20	+40	+50
	LOW	0	+4	-

4.1.1 Design of general driving circuit

In this paper, EL7457 produced by Intersil in the USA is applied to achieve the conversions of output signals.

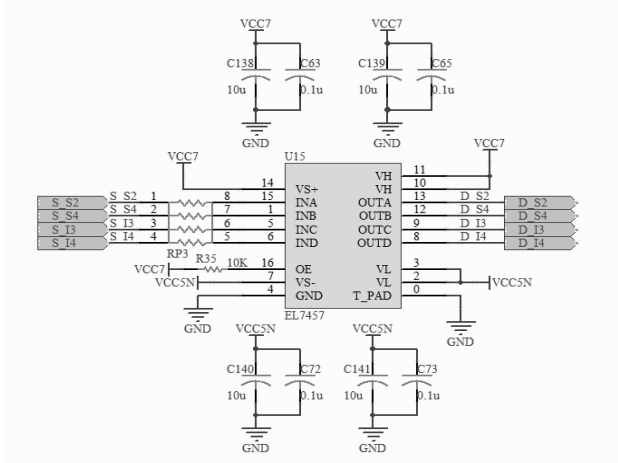

Figure 3. General driving circuit

EL7457 is featured by 4 channels, 8V ≥ VLOW ≥ -5V, -2V ≤ VHIGH ≤ 16.5V, 2A peak drive and

clocking that speeds up to 40MHz, which completely meet the requirements of normal driving signals.

As shown in Figure 3, S2, S4, I3 and I4 are four vertical transferring signals, and the chip converts 4 timing signals into power driving signals with a high level of +7V and a low level of d -5V at the same time.

4.1.2 High-voltage multiplication driving circuit

The high-level voltages of the high-voltage multiplication driving signal is adjustable and divided into 32 levels ranging from 20V to 48V in the design. The schematic of high-voltage power supply circuit is shown in Figure 4.

A voltage supply of 50V is supplied to the LT3012, i.e. a high-voltage LDO (Low Dropout Regulator), and the commands from FPGA control the resistance of MAX5435 (Digital Potentiometer), and thus change the output voltage of LT3012. For the low-voltage power supply circuit, LT1118 is adopted, which has functions of current source and current sink, in order to keep the low voltage stable. In the pulse shaping circuit, the comparer MAX999 converts the TTL from FPGA into the square signal with a peak-peak value of 5V, which subsequently improves the driving power through SN74LVC2T45, and finally controls the open or close of the push-pull MOSFET to achieve the electric multiplying function of EMCCD.

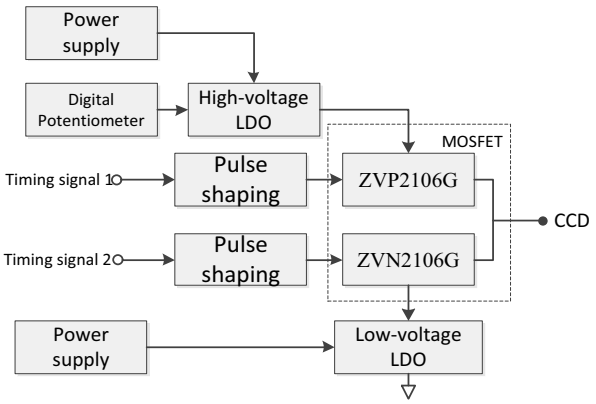

Figure 4. High-voltage multiplication driving circuit

The Class A push-pull driving amplifier circuit is shown in Figure 5. ZVP2016G and ZVN2106G, a pair of matched MOSFET (Metal Oxide Semiconductor Field Effect Transistor), are utilized to establish the circuit. The ZVP2106G has the following parameters: V_{DS}= -60V ,I_D=-450mA and $V_{GS(th)}$>0.8V; as for ZVN2106G, V_{DS}=60V, I_D=710mA and $V_{GS(th)}$<-1.5V. When no signal is input into HV_A, the voltage is about 1.4V on 1SS226 and approximately 0.7V on 1SS193. Hence, V_{GS} is about 0.7V [10] and the P-type MOSFET is pinch-off. When the signal enters into HV_A, the voltage of high level is clipped by 1SS193; the low level makes the voltage of source electrode lower than V_{GS}, so that P-type MOSFET is on and the HV_OUT outputs high level. Similarly, the signal of HV_B can control the output of low level. If to control HV_OUT of high level and low level is to generate alternation, the driving circuit would output the high-voltage multiplication driving signal.

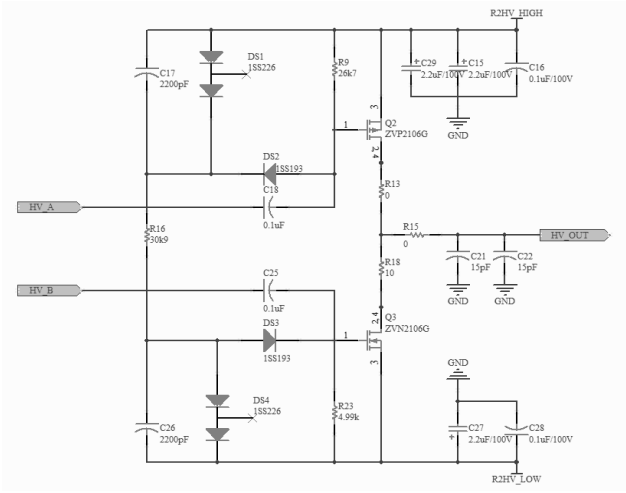

Figure 5. Class A push-pull driving amplifier circuit

4.2 Software part

The timing signals are generated from FPGA, the code of which is programmed in Verilog on the platform of XILINX ISE 14.7. The frequency of system clocking is 200MHz, and the cycle 5ns. Under this condition, the timing signals can adjust phase position and duty ratio in 5ns, before the signals go through the circuit practically. The simulation waveforms of timing signals are shown in Figure 6.

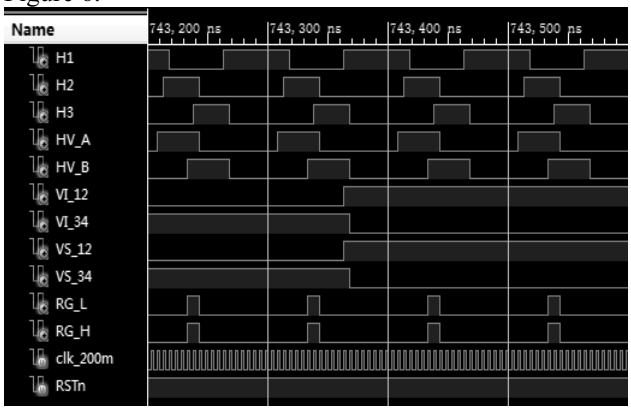

Figure 6. Simulation waveforms of timing signals.

HV_A and HV_B are the control signals of high-voltage multiplication driving circuit. If the pair of MOSFETs are on at same time, the low impedance path forms to cause the great loss of current, and even lead to a burning. In consequence, the phase relationship of HV_A and HV_B should be controlled strictly. In order to prevent the pair of MOSFETs from turning on simultaneously, the duty ratio of HV_A and HV_B should be adjusted to reduce the turn-on time of MOSFETs, which decreases the power dissipation and improves the stability of system.

5 Result and conclusion

From Figure 7, it can be seen that the high-voltage multiplication driving signal generated by the driving system has a voltage amplitude of 46V and a frequency of 10MHz, which satisfies the driving requirements of CCD97 according the design scheme.

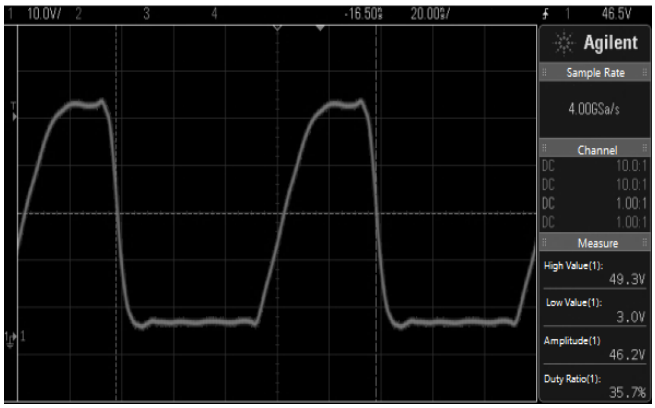

Figure 7. High-voltage multiplication driving signal

Figures 8-10 are the images shot by the camera when the high-level voltages of high-voltage multiplication driving signals are 30V, 40V and 48V respectively. The image signals which have gained correct multiplication constitute the distinct images, the details of which are clearly visible.

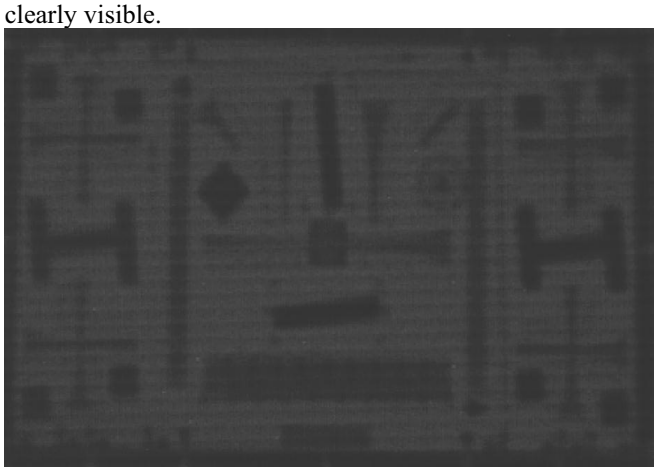

Figure 8. Obtained image at a multiplying high voltage of 38V

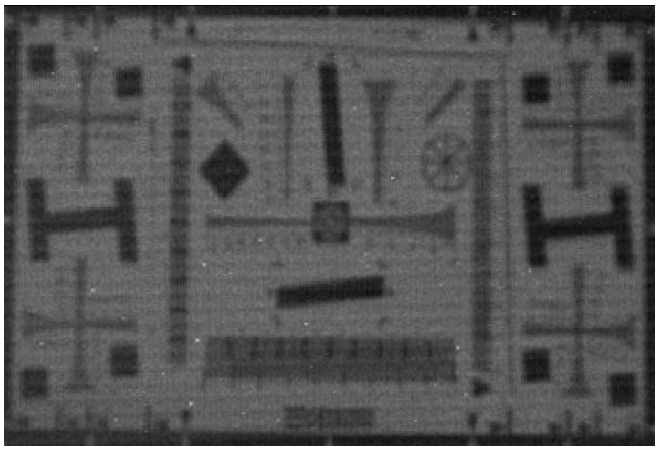

Figure 9. Obtained image at a multiplying high voltage of 40V

Figure 10. Obtained image at a multiplying high voltage of 43V

In the low-light conditions of 10^{-3} lux which requires an output clocking of 10MHz and a frame rate of 25fps, the underwater low-light camera captures the distinct pictures with a low noise. In consequence, the design of the whole driving system is successful, which meets the requirements on underwater low-light camera capturing images.

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