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# Analyzing the effect of gate dielectric on the leakage currents

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**Abstract.** An analytical threshold voltage model for MOSFETs has been developed using different gate dielectric oxides by using MATLAB software. This paper explains the dependency of threshold voltage on the dielectric material. The variation in the subthreshold currents with the change in the threshold voltage sue to the change of dielectric material has also been studied.

***Index Terms*****—** threshold voltage, gate dielectric oxides, subthreshold currents

## 1 INTRODUCTION

Earlier the VLSI designers were mainly concerned about the performance and miniaturization of the VLSI devices. For the last few years, power dissipation has been a serious issue because of the significant growth in portable computing and wireless communication. For more than 40 years, silicon dioxide has been used as dielectric because of its manufacturability and providing a continuous improved transistor performance as it is grown thinner and thinner [1-2]. The scaling of gate dielectric is done to improve the MOS transistor performance. The continuous scaling down of physical thickness of the gate dielectric and gate length has improved device performance and increased packing densities. Because of continuous scaling, the silicon dioxide dielectric thickness has been reduced to such an extent that further scaling will lead to increase in poly-Si gate depletion, gate dopant penetration, power consumption, etc. [2-4].

According to the prediction of the International Technology Roadmap for Semiconductors (ITRS) (Figure 1)[6], if the gate- oxide thickness becomes less than 1.4 nm for sub- 100 nm MOS then it results in the direct tunneling current. This tunneling current increases with the reduction of gate- oxide thickness and hence, the static power dissipation also increases [3-5]. It can be observed from the figure that even with the conservative equivalent oxide thickness scaling, excessive gate leakage prohibits continued gate- dielectric scaling using silicon- dioxide and thus it is required to find an accurate replacement of silicon dioxide such as high- k dielectric materials (Figure 2).

Basic material properties which are important for the selection of alternative gate dielectric are dielectric permittivity, band gap, band alignment with respect to silicon, thermodynamic stability, film morphology and uniformity, interface quality, and reliability [4].

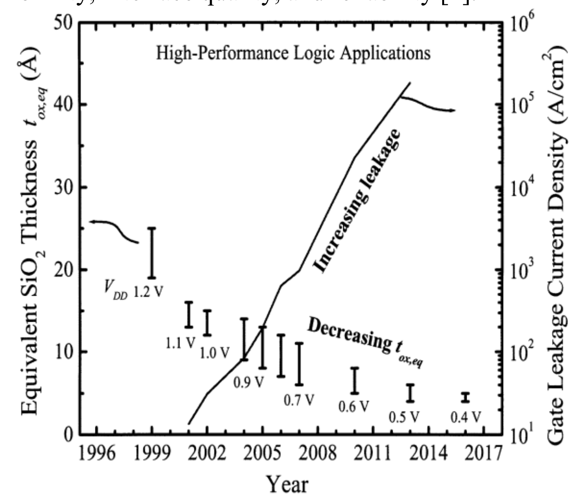


**Figure 1** Scaling trend of the MOSFET gate dielectric thickness. The projected range of equivalent $SiO_2$ thickness for high- performance logic applications is plotted using bars. The supply voltages are also indicated and the largest value for each bar, the gate- leakage current density through $SiO_2$ is calculated and plotted as solid line [6].

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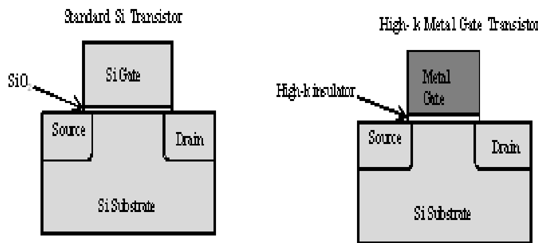


**Figure 2**. MOS Transistor Structure with Dielectric Gate [7]

Figure 3 presents dielectric constants of some of the high- k candidates:

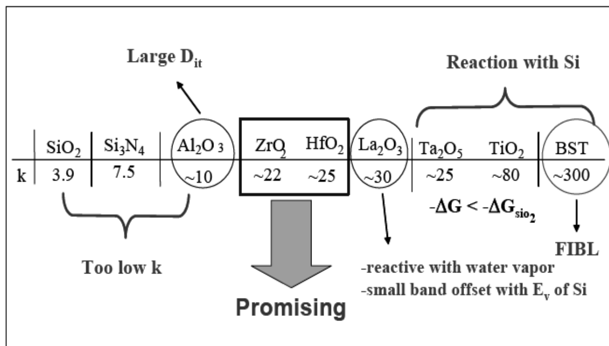


**Figure 3.** Dielectric constants of some high-k dielectrics [8]

### 1. SOURCES OF LEAKAGE POWER

Four sources of leakage currents are described as follows (Figure 4) [9]:

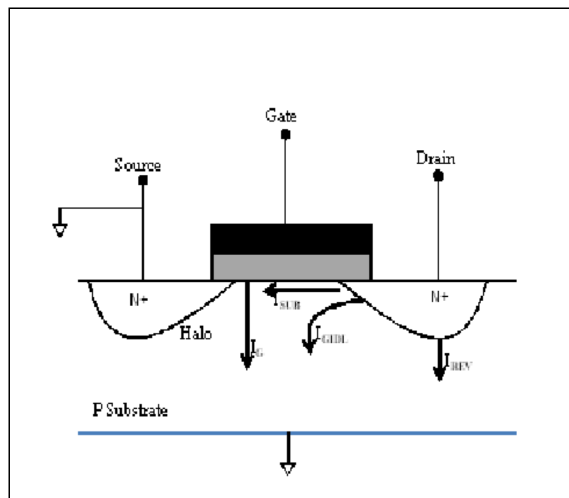


**Figure 4.** . Leakage current components in an NMOS transistor [9]

*A. Reverse- biased junction leakage current ($I_{REV}$)*

When a transistor is off, the leakage takes place from the source/ drain to the substrate via the reverse- biased junctions. For an NMOS transistor, in off- state, $V_{DS}$ is equal to the supply voltage which results in the flow of leakage current. The magnitude of leakage current depends upon the drain diffusion area and the leakage current density determined by the doping concentration.

*B. Gate Induced Drain Leakage ($I_{GIDL}$)*

The leakage occurs due to the high field effect in the drain junction. In the case of an NMOS, when the gate is grounded and drain potential is at $V_{DD}$, electron-hole pair generation takes place through avalanche multiplication and band- to- band tunneling because of band bending in the drain. The holes get swept out to the substrate which causes a serious depletion condition, at that very instant electrons get collected in the drain causing a flow of GIDL current. GIDL current increases with an increase in the $V_{DS}$ and $V_{DG}$.

*C. Gate direct- tunneling Leakage ($I_G$)*

The leakage current flows from the gate via the leaky oxide insulation to the substrate. In thick oxides (greater than 3-4 nm), leakage results due to the Fowler-Nordheim tunneling of electrons in the conduction band of the oxide layer on the application of a high electric field across the oxide layer. Whereas for thin oxides (in 0.15μm and less), direct tunneling through the oxide layer is the major problem. The magnitude of direct tunneling current exponentially increases with the oxide thickness ($T_{ox}$) and supply voltage ($V_{DD}$).

*D. Subthreshold (weak inversion) Leakage ($I_{SUB}$)*

The drain- source current, flowing when the transistor is operating in the weak inversion region, is the leakage current. Subthreshold conduction occurs due to the diffusion current of the minority carriers in the channel. The magnitude of subthreshold current is a function of the temperature, supply voltage, device size, and the process parameters of which the dominant role is played by the threshold voltage.

## 2 EXPERIMENTAL WORK

The fabrication of MOS capacitors is done on 200mm n- and p- type Si substrates. The basic structure of a MOS transistor is shown in Figure 2. Different high-k dielectric materials have been investigated to replace silicon dioxide as the gate dielectric material. The amount of variation in the subthreshold current with the threshold voltage has been calculated using MATLAB. In addition, the effect of interface trap charges, doping concentration and also oxide thickness on the threshold voltage for NMOS and PMOS has been observed. The oxide thickness is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. The interface trap charge is kept at $5*10^{10}$ qC/cm$^2$ and the doping concentrations ($N_a$, $N_d$) are varied from $10^{15}$cm$^{-3}$ to $10^{16}$cm$^{-3}$ respectively. The threshold voltage versus oxide thickness for various doping concentrations at the constant interface trap charge ($Q_i = 5*10^{10}$qC/cm$^2$) for various dielectric materials such as silicon dioxide ($SiO_2$, k = 3.9), aluminium oxide ($Al_2O_3$, k = 10), hafnium oxide ($HfO_2$, k = 23) and tantalum oxide ($Ta_2O_5$, k = 25) have been plotted. All calculations have been done considering the MOS capacitor to be at room temperature (T = 300K).

## 3 Results and discussion

From the results, it can be seen that the threshold voltage for NMOS and PMOS are positive and negative respectively. The threshold voltage for NMOS becomes more positive with the increase in the oxide thickness whereas in the case of PMOS, the value of threshold voltage becomes more negative. Threshold voltage also varies with the dielectric constant. The larger the dielectric constant of the gate-dielectric material, the more is the threshold voltage. Threshold voltage is being calculated as

$$V_{th} = \varphi_{ms} - \frac{Q_{fc}}{C_{ox}} + \frac{2kT}{q} ln\left(\frac{N_a}{N_i}\right) + \sqrt{\frac{2\epsilon_{Si}\, qN_a\, (2\varphi_b + V_{sb})}{C_{ox}}}$$

where $\varphi_{ms}$ is the metal semiconductor work function and can be calculated as the difference of work function of metal and the substrate ($\varphi_m - \varphi_{Si}$), $N_a$ and $N_d$ are the doping concentrations, $C_{ox}$ is the oxide capacitance $V_{sb}$ is the substrate bias voltage.

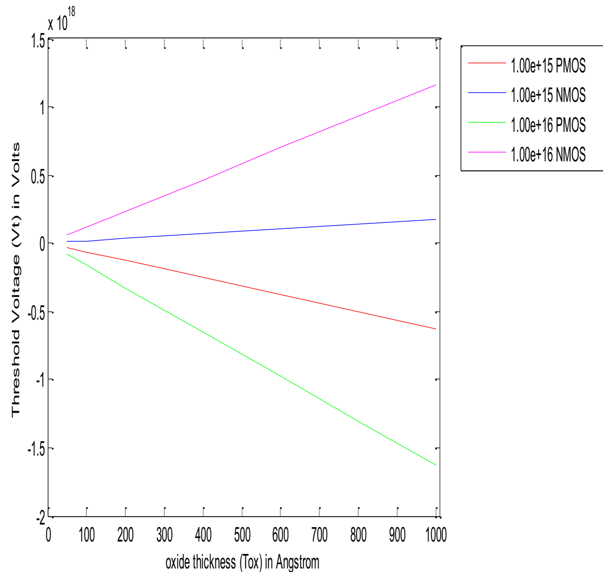


**Figure 5** Plot showing $SiO_2$ thickness versus Vth

From Figure 5, it is evident that with the increase in oxide thickness, the threshold voltage for NMOS becomes more positive and that for PMOS becomes more negative.

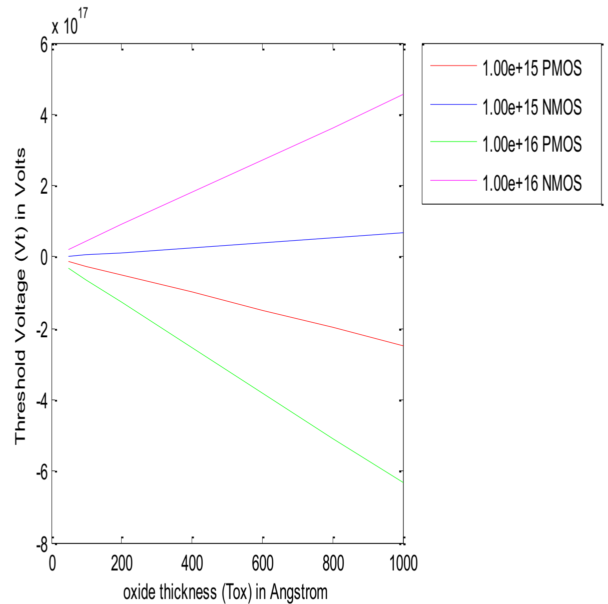


**Figure 6.** Plot showing $Al_2O_3$ thickness versus Vth

From Figure 6, it can be observed that for aluminium oxide, the dependency of the threshold voltage on the oxide thickness is same as that in the silicon dioxide but the value of threshold voltage is less as compared to that for silicon dioxide.

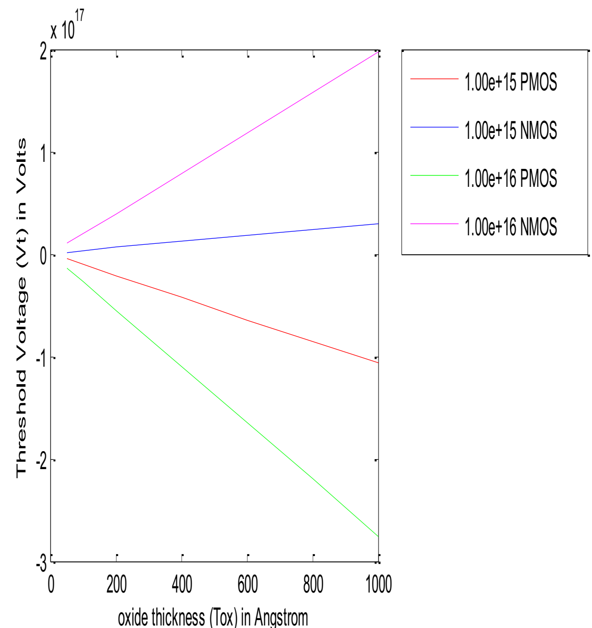


**Figure 7.** Plot showing $HfO_2$ thickness versus Vth

The threshold voltage for hafnium oxide is further lesser than that for aluminium oxide.

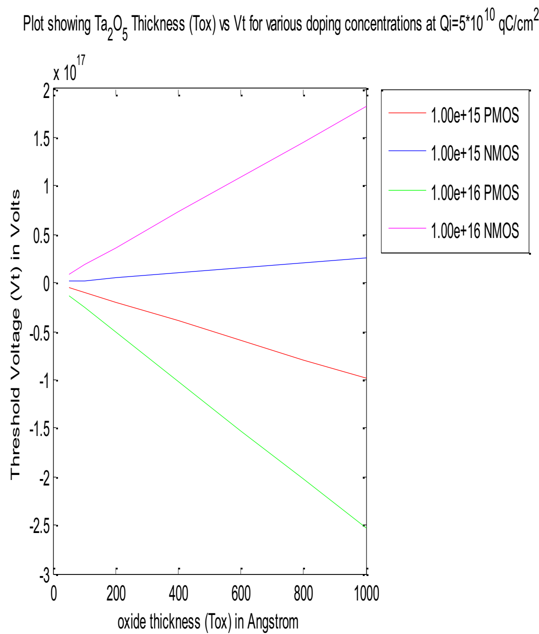


**Figure 8.** Plot showing $Ta_2O_5$ thickness versus Vth

On comparing the threshold voltages of all the above cases, it has been found out that the threshold voltage for tantalum oxide is the minimum.

Hence, it has been justified that with the increase in dielectric thickness, and dielectric constant the threshold voltage of the MOSFET decreases.

The subthreshold current can be calculated as

$$I_{sub} = I_0 \, e^{\left[\frac{V_{gs}-V_{th}}{nV_t}\right]} \left[1 - e^{\frac{-V_{ds}}{V_t}}\right]$$

where $V_{gs}$ is the gate-to- source potential, $V_{th}$ is the threshold voltage, n is the subthreshold swing coefficient [= $dV_g$ /d($\log I_d$)], $V_t$ is the thermal voltage [=kT/q], $V_{ds}$ is the drain- to- source potential. The Table 1 hereby provides the values for the subthreshold current at a certain threshold voltage for a particular dielectric material in a PMOSFET. The values have been calculated at various oxide thicknesses in Angstrom (Å) 50, 100, 200, 400, and 600.
From the table 1, we have justified that in the case of PMOSFET; with the increase in the oxide thickness the threshold voltage becomes more negative (i.e. decreases) while the subthreshold current increases. On the other hand, we also observe that with the increase in the dielectric constant of the gate dielectric oxide material, the threshold voltage becomes more positive (i.e. increases) while the subthreshold current decreases. But in the case of NMOS, with the increase in oxide thickness, the threshold voltage becomes more positive (i.e. increases) and so the subthreshold current decreases.

**Table 1** Subthreshold current for the corresponding threshold voltages for a particular dielectric material in a P-MOSFET

| $T_{ox}$ (Å) | Threshold Voltage (Vth in Volts) | | | Subthreshold Current ($I_{SUB}$ in A) | | |
|---|---|---|---|---|---|---|
| | $SiO_2$ (3.9) | $Al_2O_3$ (10) | $HfO_2$ (23) | $SiO_2$ (3.9) | $Al_2O_3$ (10) | $HfO_2$ (23) |
| 50 | -0.3165 | -0.1234 | -0.0537 | 4.01 x $10^{48}$ | 6.38 x $10^{46}$ | 1.43 x $10^{46}$ |
| 100 | -0.6330 | -0.2469 | -0.1073 | 1.78 x $10^{51}$ | 4.5 x $10^{47}$ | 2.26 x $10^{46}$ |
| 200 | -1.2659 | -0.4937 | -0.2147 | 7.02 x $10^{56}$ | 8.08 x $10^{58}$ | 1.13 x $10^{47}$ |
| 400 | -2.6318 | -0.9874 | -0.42933 | 2.17 x $10^{68}$ | 8.90 x $10^{53}$ | 5.63 x $10^{48}$ |
| 600 | -3.7977 | -1.4811 | -0.6440 | 9.03 x $10^{79}$ | 2.37 x $10^{58}$ | 3.77 x $10^{50}$ |

## 4 CONCLUSION

The scaling of the silicon dioxide has reached to an extent that on further scaling there will be an increase in the leakage currents. That is why there is a need for the replacement of silicon dioxide with another material. The possible material can be a high-k dielectric material provided it possesses the basic material properties like dielectric permittivity, band gap, band alignment with respect to silicon, thermodynamic stability, film morphology and uniformity, interface quality, and reliability. The various candidates high- k dielectric materials considered are $Si_3N_4$ (~7.5), $Al_2O_3$ (~10), $ZrO_2$ (~22), $HfO_2$ (~25), $La_2O_3$ (~30), $Ta_2O_3$ (~25), $TiO_2$ (~80), and BST (~300). Out of these the most reliable materials are $ZrO_2$ and $HfO_2$. High- k dielectric materials are required to reduce the leakage currents. Four different leakage current sources have been studied but we have counted upon the variation of subthreshold currents with respect to the change in the threshold voltage along with the oxide thickness and dielectric constant. The results justify the need of the adoption of high-k dielectric materials.

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