Design and analysis of single- ended robust low power 8T SRAM cell

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Abstract. This paper is based on the observation of 8T single ended static random access memory (SRAM) and two techniques for reducing the sub threshold leakage current, power consumption are examined. In the first technique, effective supply voltage and ground node voltages are changed using a dynamic variable voltage level technique(VVL). In the second technique power supply is scaled down. This 8T SRAM cell uses one word line, two bitlinesand a transmission gate. Simulations and analytical results show that when the two techniques combine the new SRAM cell has correct read and write operation and also the cell contains 55.6% less leakage and the dynamic power is 98.8% less than the 8T single ended SRAM cell. Simulations are performed using cadence virtuoso tool at 45nm technology.

1 Introduction

With the large usage of static random access memory in integrated circuits for high density and stability, thedemand for SRAM is increasing [1]. Low power circuits demand is increasing rapidly not only for logic circuits but also for storage elements. So power consumption of SRAM cells must be reduced. In this paper 8T SRAM cell is proposed to reduce theleakage, static, and dynamic power at circuit level. There are numerous techniques to reduce the standby power. One is to use sleep technique in which standby power is reduced by disconnecting the supply voltage from the cell using high threshold voltage pMOSFET and disconnecting the ground path by using high threshold nMOSFET[2].However, this has serious limitation of high increase in sub threshold leakage current because of its exponential relation with threshold voltage. So to solve this problem a dynamic variable voltage level technique that can significantly reduce the power dissipation, leakage current is proposed. The present work describes the use of this technique to reduce the supply voltage and to increase the ground level potential for yielding the maximum reduction in leakage currents and power dissipation [3].

In this paper we propose a 8T SRAM cell at 45nm technology, this cell is composed of eight transistors in which two inverters are cross coupled(M1, M2, M3, M4), transistors M5 and M6 are access transistors, M7 and M8 are read access transistors forming a transmission gate.

The organization of the paper is as follows: Sect2 describes the proposed 8T SRAM cell and the read and write operation. Section 3 describes the leakage current that flows in this circuit and the power dissipation.Section 4 describes the various techniques. Section 5 gives the brief conclusion.

2 Read and Write operation of circuit

The proposed 8T SRAM cell has three modes of operation i.e. write mode, read mode, hold mode. Write operation starts by cutting off the transmission gate connection from the circuit .Then the data which needs to be written is placed on the BL and complement of the data is placed on the BLBAR .Q and Qb are two storage nodes.M1 and M2 are pull up pmos transistors and M3 and M4 are pull down transistors. Word line is responsible for holding the data in active and hold mode. The SRAM cell looks like two cross coupled inverters,inv1 followed by inv2.The output of the first inverter becomes the input to the second and vice versa. In this cell a transmission gate is used to read the data.RWLB is inversion of RWL signal .When both RWL and RWLB are assertedand once the transmission gate gets on, the stored data at node Q gets transferred and is read[4].

One of the major advantages of transmission gate is that it eliminates the requirement of sense amplifier and precharge circuit as used in conventional 8T SRAM cell for the read purpose thus lowering the power

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consumption of the cell [10]. Figure 1 shows the schematic of 8T SRAM cell.

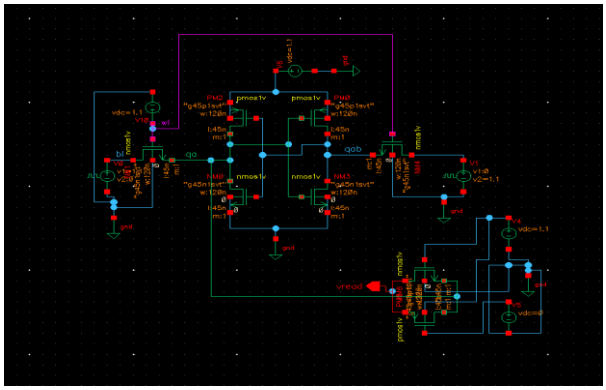

Figure 1. Schematicof 8T SRAM cell

2.1 Read and write waveforms

Read operation: During the read operation the data stored at Q node is passed to the input of the transmission gate where both the word lines RWL, RWLB are asserted. Then the output is taken from read path rout.

Write operation: During the write operation the data that needs to be written is placed is at Bit Line and its complement on BLBAR. WL is asserted high after that.

Hold mode: During hold the WL remains off and cell is in idle state [5]. The output waveforms for write and read operation are shown in Fig.2 and 3

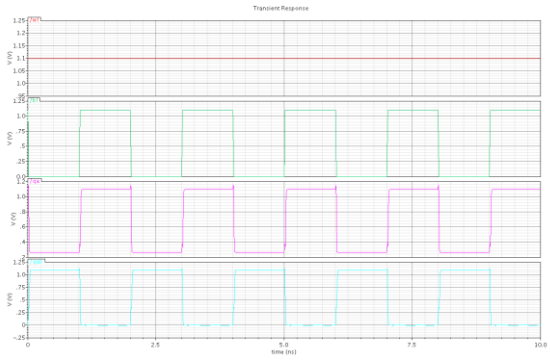

Fig2. Write operation

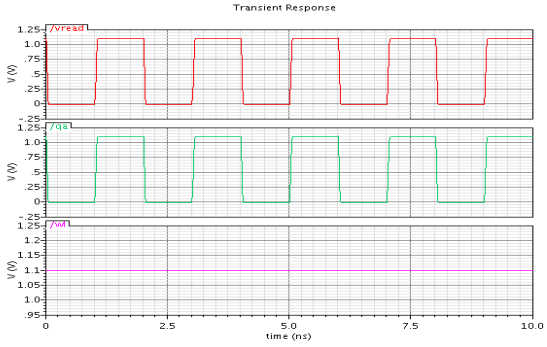

Fig 3. Read Operation

3 Leakage Current

There are various contributors that give rise to leakage currents like pn junction Reverse Bias current, Sub threshold leakage, drain induced barrier lowering, Body-effect, Tunneling into and through gate oxide, Injection of hot carriers, Gate induced Drain Leakage, Punchthrough.But the main contributor to leakage current is Sub thresholdleakage. Sub threshold currentis that current that flows between source and drain terminal in an MOS transistor when the gate voltage is belowthe threshold voltage. Leakage current can be obtained from the equation below when transistor is in off state [6].

$$I_{sub}=I_{oe}\frac{vgs-vth+\eta vds-\gamma vsb}{nV\theta}(1-e^{\frac{-Vds}{V\theta}}) \quad (1)$$

where, $I_o= \mu C_{ox}(w/l_{eff})V_\theta^2 e^{1.8}$,W= width, L= length, μ = carrier mobility,V_θ is thermal voltage,η is drain induced barrier lowering coefficient, n is sub threshold swing coefficient.V_{TH} is threshold voltage, V_{GS} is gate to source voltage.

3.1 Leakage current is calculated for that particular transistor which is in off condition during the time of operation.

A) To write 1 at Q node

For writing 1 in Qnode, transistor M2 and M3 will be off so we will take leakage current from these two nodes.

Leakage current at M2 transistor=4.27 pA

Leakage current at M3 transistor=-10.43 pA

B) To write 0 at Q node

For writing 0 in Q node, transistor M1 and M4 will be off so we will take leakage current from these two nodes.

Leakage current at M1 transistor=5.66 pA

Leakage current at M4 transistor=-5.57 pA

Leakage currents for writing 0 are shown in Fig.4

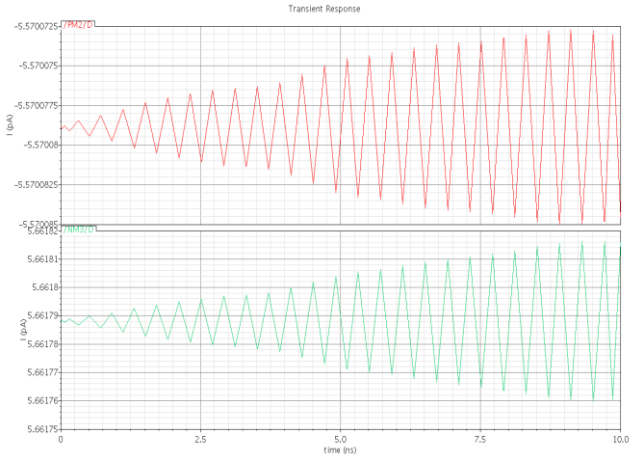

Fig 4. Leakage currents for write '0' at Q node

3.2 Power Dissipation

Power dissipation of SRAM cell is the sum total of static and dynamic power dissipation. Static power dissipation occurs due to leakage currents [7].

Dynamic power dissipation is of following types:

a) Switching: Due to the charging and discharging of current that results from the parasitic capacitances.
b) Short circuit: Due to the slow change of inputs i.e. when both the pmos and nmos are on in an inverter this results in short circuit dissipation

Dynamic power dissipation is calculated by giving vpulse on both the bit lines and word line is asserted and doing the transient analysis at 45nm technology [8].

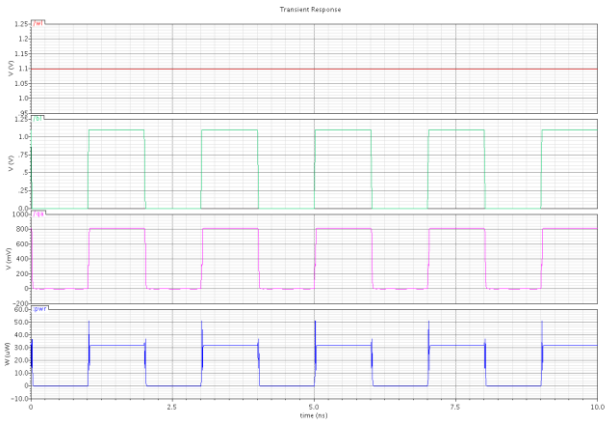

Fig 5. Dynamic Power Dissipation

4 Leakage current and power dissipation control techniques

4.1 Dynamic variable voltage level technique

In this technique supply voltage is not directly connected to the SRAM cell instead a upper dynamic voltage is set using one pMOS connected in parallel with series of two nMOS transistors. Also the ground potential is increased using one nmos connected in parallel with series of two pmos[9].This technique gives '0' Volt at ground node during the active mode and an increased ground voltage during the standby mode. At upper voltage node the technique gives full voltage Vdd in active mode, while the supply voltage is reduced to level Vd in the stand-by mode.

Simulation results showing the reduction in leakage currents are shown in Fig. 6 and Fig. 7

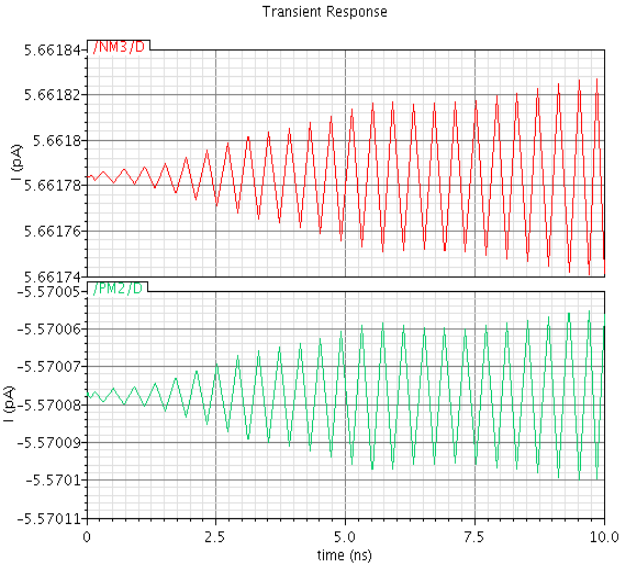

Fig 6. Leakage current for write '0'

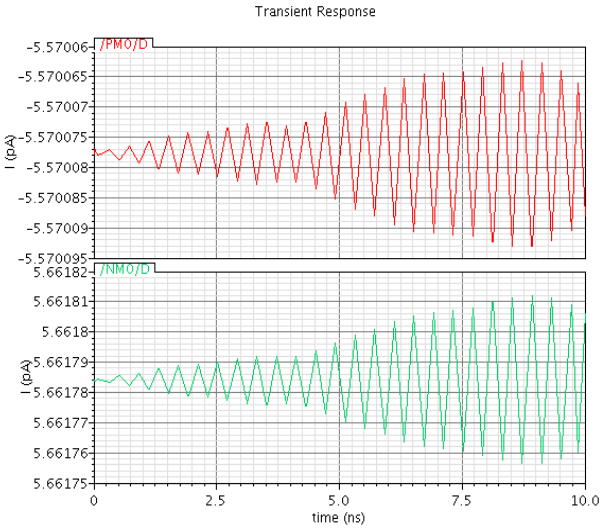

Fig 7. Leakage current for write '1'

Simulation results showing the reduction in power dissipation is shown in Fig. 8

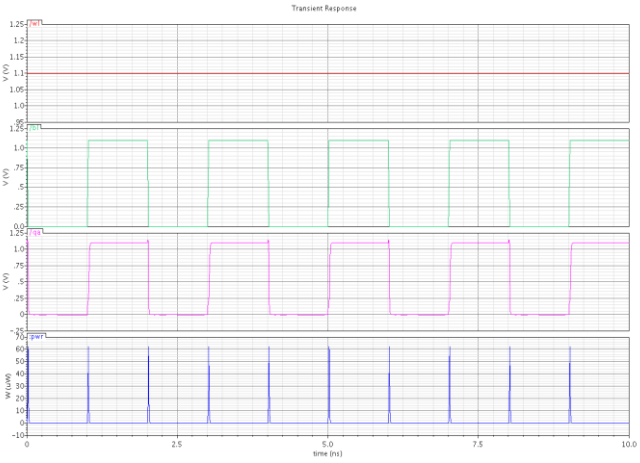

Fig.8 Dynamic Power Dissipation

4.2 Power supply scaling combined with dynamic variable voltage level technique

Fig 9 shows the schematic of the combined technique in which the power supply is lowered to 0.7V.

Fig 10 and 11 shows the leakage currents.

Fig 12 shows the dynamic power dissipation.

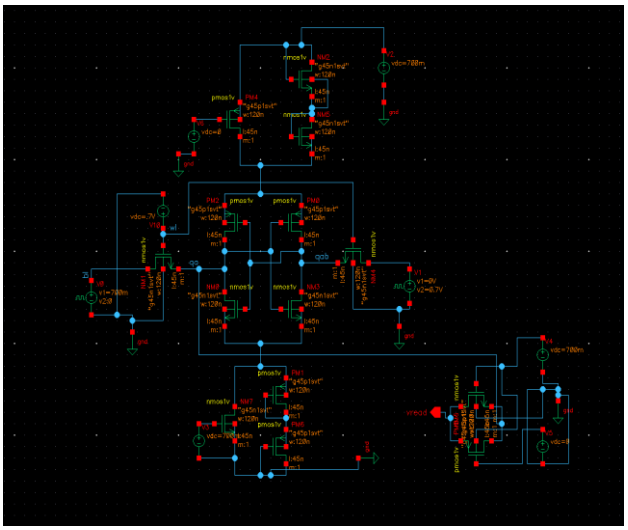

Fig 9. Schematic of proposed cell

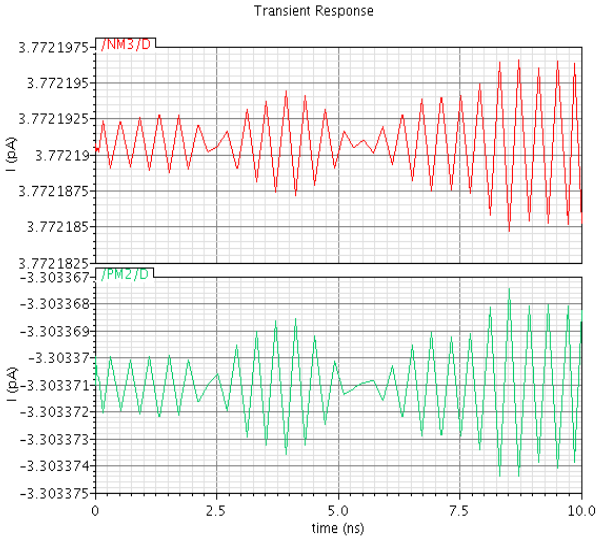

Fig 10. Write '1' leakage current

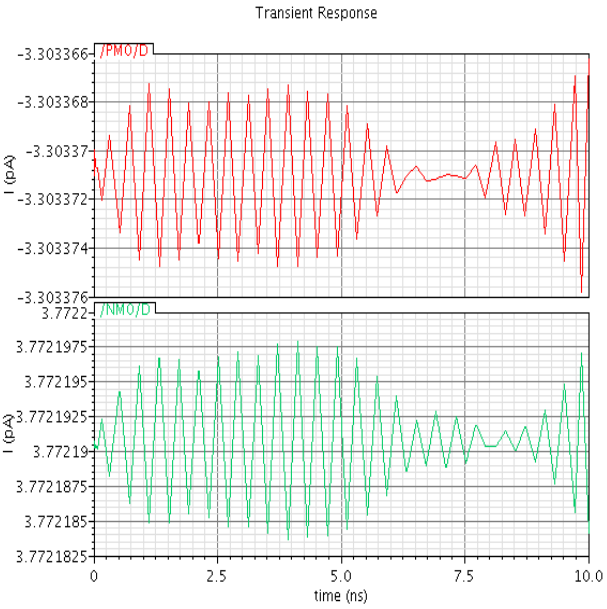

Fig 11. Write '0' Leakage Current

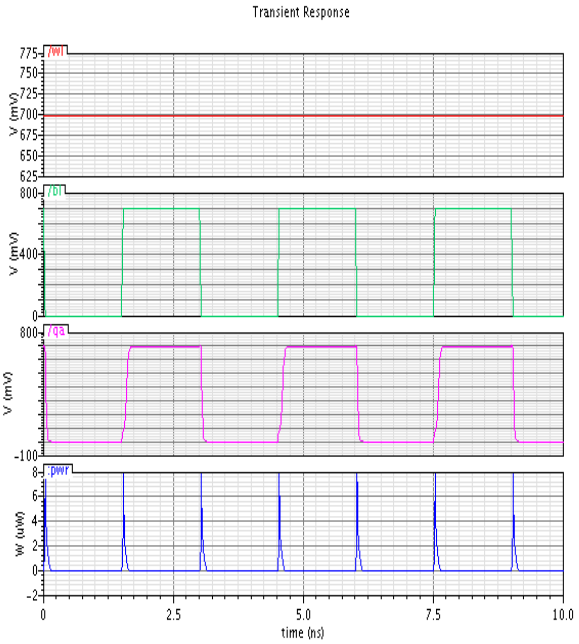

Fig 12. Dynamic Power Dissipation

Table 1 shows the comparison between the conventional 8t SRAM cell and the two techniques proposed. Total power dissipation of the proposed structure shows 98.8% reduction in comparison to conventional 8T and this is due to the power supply scaling combined with dynamic VVL technique.

Table 2 shows the comparison between the leakage currents.

Table 1. Comparison in terms of Dynamic PD

Power Dissipation	**Conventional 8T SRAM**	**SVL technique**	**Power scaling combined with SVL technique**
Static	3.19 uW	32.1 pW	8.42 pW
Dynamic	16.1 uW	736.3 nW	181nW

Table 2. Comparison in terms of Leakage currents

Leakage current	**Conventional 8T SRAM**	**SVL technique**	**Power scaling combined with SVL technique**
Write'1' (nmos, pmos)	4.27 pA, -10.43 nA	5.66pA, -5.57 pA	3.3 pA, -3.3 pA
Write0'(nmos, pmos)	5.66 pA, -5.77 pA	5.66pA, -5.57 pA	3.3 pA, -3.3 p A

5 Conclusion

As the CMOS technology is scaling down to 45nm, power dissipation has become a very crucial issue in the VLSI design. In this paper a low power single ended 8T SRAM cell has been proposed An analysis of leakage current and power dissipation in 8T SRAM cell for 45nm technology shows that leakage currents contribute significantly to the total power dissipation in standby mode. Reducing the voltage supply and increasing the voltage at ground node using dynamic VVL technique for the reduction in leakage currents are examined in detail. It was analyzed that scaling down the supply voltage with the VVL technique gives significant reduction in both static and dynamic power dissipation for write operations. Although delay and area have increased in the proposed SRAM cell but low power dissipation can dominate over this drawback. So, this proposed SRAM cell can be used in wide applications as to provide low power benefits in laptops, mobile phones, memory cards etc. So we can conclude that these techniques have significantly reduced the leakage currents and power dissipation in 8T SRAM cell.

Acknowledgments

This work was done was in CDAC, Mohali by using cadence virtuoso tool.

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