Design and analysis of 32 bit CMOS adder using sub-threshold voltage at deep submicron technology

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Abstract. FA is basic cell for arithmetic operation and lots of efforts have put to minimize power consumption and delay. This paper evaluates conventional CMOS adder, bridge style adders in sub-threshold region. Circuits are designed at 20 MHz and 50 MHz frequencies with V_{DD}= 200 mv. All adder designs are simulated at 32 nm technology. In 1 bit and 32 bit conventional CMOS adder design, an efficient trade-off between delay and power is achieved. Experimental results show that 32 bit adder designs have significant improvements in delay and power delay product.

1 Introduction

CMOS VLSI circuits has been identified as a critical technology need in the recent years due to the high demand for low power consumption, lower delay, small area and low cost design are increasing every day. In VLSI applications, arithmetic operations play an important role in modern processing systems. Major operations of arithmetic are addition, Sub-traction, multiplication and accumulation. Full adder (FA) cell is the basic block for most of arithmetic systems. Improving the FA characteristics is critical for measuring overall system quality. In many computers and other kinds of processor, adders are not used only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operation.

Sub-threshold design is a technique for reducing dissipated power [1]. Due to portable devices; the adder must have high speed, lesser area and lower power consumption. Devices like mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. Basically full adder is the core components of microprocessor and other complex chips. So the performance of full adder would affect the system as a whole. All the circuits are designed in sub-threshold region. The main factor in sub-threshold design is maintaining a good trade-off between power consumption and performance. In recent years, considerable research has been performed on FA design with various design methodologies and different technologies [9]. In these days several Adder designs have been proposed to reduce the power consumption. Logic minimization gives better results in power consumption. For low power results it is always advisable to use CMOS technology. In paper, three different 1-bit full adder topologies in deep sub-threshold operation are proposed. The cells are characterized with respect to delay, power consumption, Power-Delay Product (PDP) and leakage power. Conventional CMOS Adder and Bridge style adders are designed at 20mhz and 50mhz frequencies with V_{DD}= 200mv.

2 Sub-threshold design

In sub-threshold circuits, the supply voltage is reduced well below the threshold voltage. Due to reduction in power with respect to supply voltage, sub-threshold circuits are classified as ultra-low-power circuits. Specifically in application areas where performance can be sacrificed for low power, sub-threshold circuits are ideal fit [11].

Some of the applications include devices such as digital watched, radio frequency identification (REID), sensor nodes and battery operated devices such as, cellular phones.Design spectrum is a trade-off between power consumption and performance. One extreme aim of this spectrum is ultra-low power while performance is of secondary importance. In this solution, circuit is biased in sub-threshold region so that standard CMOS logic is extended to operate in sub-threshold region by reducing the supply voltage V_{dd} less than transistor threshold voltage V_t . The motivation for using sub-V_t circuits is the ability to exploit the sub V_t leakage current as the operating drive current. In sub-threshold region, the reduction in power consumption outweighs the increase in delay. Thus the circuit has lower PDP when it operates in sub-threshold region. So in the same frequency, when

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the circuit operates in sub-threshold region, its energy consumption is less than when it works in supper-threshold.

3 A Review on full adder circuits

In this section, various 1-bit full Adder designs are examined. Some of these schemes are based on CMOS logic with low power consumption, good signal logic level and high driving ability.

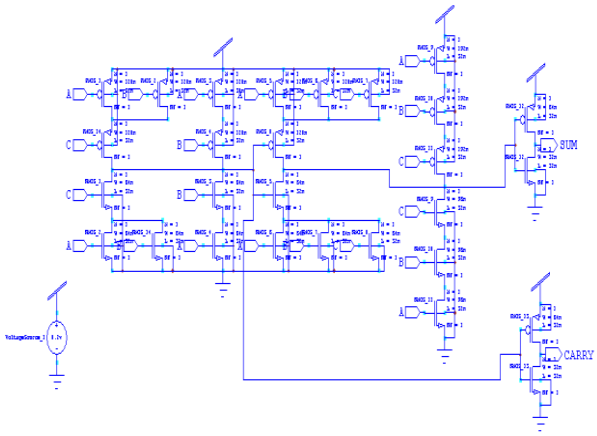

Figure 1. Conventional CMOS 1 bit full adder (CCMOS)

The schematic shown in the above fig. is CCMOS full adder [9] designed in the tanner schematic editor, which is based on regular structure CMOS logic and almost equal rise and fall time. It uses 28 transistors to complete one bit full adder. In this section bridge style 1-bit full adder introduced which operating in sub-V_t region is introduced. This can be divided into two main modules: sum module and carry module. Equations (1) and (2) show the logical functions of the full adder outputs.

$$\text{Sum} = a \oplus b \oplus c \quad (1)$$

$$\text{Carry} = a.b + b.c + a.c \quad (2)$$

Based on these equations, two implementation of full adder with bridge design are investigated. The first is shown in fig. 2 which called in this paper as Bridge_v2. This design needs 24 transistors against conventional CMOS full adder uses 28 transistors and should have complementary inputs. Third design is Bridge_v3 shown in fig. 3. These three circuits are designed and simulated at 32 nm technology. Bridge method uses some transistors, called bridge transistors, as conditional conjunction between two nodes of circuit so this method shares transistors of different paths from power supply to output.

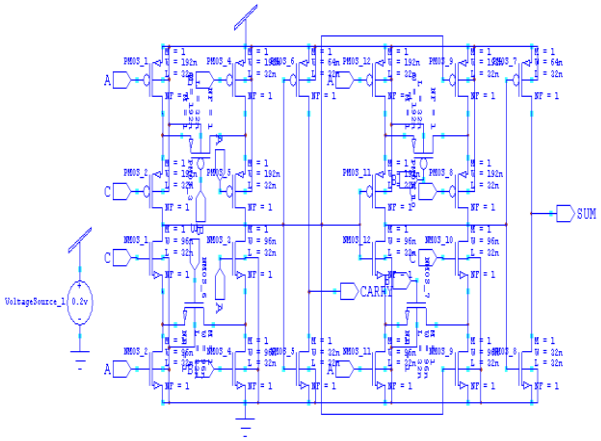

Figure 2. Bridge type (B_V2) 1 bit full adder style.

It uses 24 transistors for evaluating the sum and carry. The name itself shows that it uses bridge type structure for implementing the SUM and CARRY. It shares the path between carry and sum circuits with fully symmetric full adder structure fig 2.

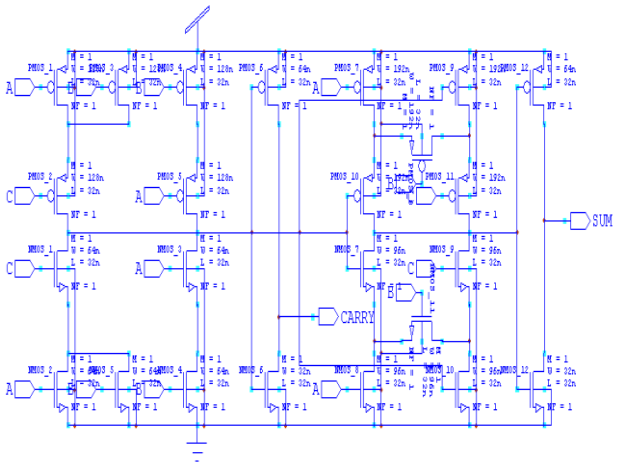

Figure 3. Bridge type (B_V3) 1 bit full adder style.

It uses 24 transistors for evaluating the sum and carry. It shares the path between carry and sum circuits with semi symmetric full adder structure fig 3.

4 Results

4.1. Results of full adder at 32 nm

Table 1 represent comparison results of 1 bit full adders. Proposed designs CCMOS, Bridge style are simulated at 20MHz and 50 MHz frequency. In this, parameters like average power consumption, delay and power delay product are measured. Our result shows improvement in average power consumption and power delay product.

Table 1. Result of 1 bit adders

Sr no	Parameters	S. Wairya et.al [6]		Farshad Moradi et.al [7]	Xu Wang et.al [8]	Proposed design [20 MHz]		
		CCMOS	BRIDGE STYLE	CMOS	CMOS	CCMOS	BRIDGE STYLE (B_V2)	BRIDGE (B_V3) semi-symmetric
1.	Technology	90nm		65nm	180nm	32nm		
2.	Average power (µw)	2.24	1.82	0.021	0.000049	0.00753	0.00881	0.00769
3.	Delay (ns)	0.524	0.323	1000	14	7.5	8.66	8.69
4.	Power delay product(fj)	1.17	0.59	21.0	694.4	0.05647	0.07629	0.06683
5.	Leakage power (nw)	_	_	_	_	2.127	2.422	2.132

In table 2 all the circuit designs are simulated at 50 MHz frequency. In this, parameters like average power consumption, delay and power delay product and leakage power are measured.

Table 2. Result of 1 bit adders at f= 50 MHz

Sr. No	Name of adders	No. of transistor	width	Delay(ns)	Avg. power (nw)	Power delay product (aj)	Leakage power (nw)
1.	CCMOS	28	W*4	5	13.99	69.95	2.127
2.	B_V2	28	W*4	5.91	18.74	110.75	2.422
3.	B_V3	28	W*4	5.94	13.46	79.95	2.132

Table 3 represent comparison results of 32 bit Ripple Carry adders. All the circuit designs are simulated at 50 MHz frequency. Proposed design has improvement in delay and power delay product.

Table 3. Result of 32 bit Ripple Carry adders

Sr. no	Parameters	Mohammad Reza Bagheri.et.al [9]			Proposed design [50 MHz]		
		CCMOS	BRIDGE STYLE (B_V2)	BRIDGE STYLE (B_V3)	CCMOS	BRIDGE STYLE (B_V2)	BRIDGE STYLE (B_V3)
1.	Average power (µw)	0.190	0.063	0.063	1.554	1.654	1.480
2.	Delay (ns)	43.66	65.00	50.35	2.539	2.681	3.251
3.	Power delay product (fj)	8.320	4.112	3.189	3.946	4.434	4.811
4.	Leakage power (µw)	_	_	_	0.657	0.769	0.685

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4.2 Simulation Result

Simulation waveform of CCMOS is shown in fig 4.The input data V_a, V_b, V_c and output sum and carry shown below:

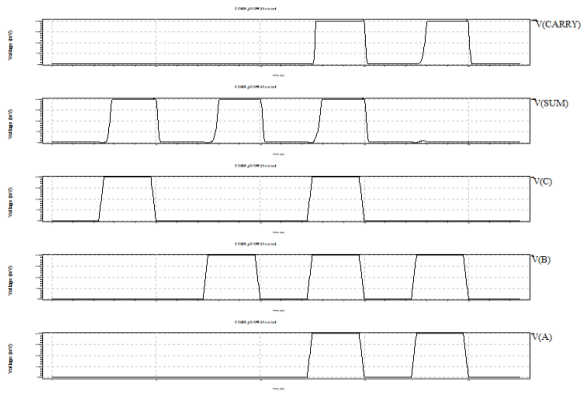

Figure 4. Output Waveform of CCMOS Simulation

5 Conclusion

The aim of this paper is reduce the power consumption. In this paper CCMOS design and bridge style adders are compared in sub-threshold region. Results show that significant improvements in power consumption, delay and power delay product with acceptable performance. All the adder circuits are designed at 20 MHz and 50 MHz frequencies with V_{DD}= 200mv. All adder designs are simulated at 32 nm technology.

In 1 bit Conventional CMOS adder, average power is improved by 99.66% and power delay product is improved by 95.17%. In Bridge Style adder, average power is improved by 99.51% and power delay product is improved by 87.07%.

In this paper circuits make use of 50MHZ frequency; then our result is improved. In 32 bit Conventional CMOS, delay is improved by 94.18% and power delay product is improved by 52.58%. In Bridge style (B_V2) design, delay is improved by 95.87%. In Bridge style (B_V3), delay improved by 93.54%.

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