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Non-contact wafer thickness measurement of capacitance sensor circuit based on CAV424

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Abstract: Non-contact wafer thickness measurement with the CAV424 capacitance sensor special integrated circuit and arc pole plate capacitor sensor has good stability and linearity under low capacity of the bottom of sensor and low ⊿C condition. This method has a high technical advantages and practical value.Two capacitance sensors Cb, Ca measurement spacing 4mm install at the same axis which constitutes the size condition for measuring thickness. The static capacity of Ca and Cb is a constant value. The capacity of Cb and Ca will change when the silicon wafer is involved. This change is checked by the CAV424 capacitive sensor which has better linearity and higher thickness resolution.

Key words: Circular planar capacitance sensors; CAV424 application-specific integrated circuit for capacitance sensor; Application design and non-contact thickness test.

INTRODUCTION

Semiconductor silicon non-contact thickness measurement has higher difficulty and practical value. Since the silicon ingot cutting with a silicon wafer has the thickness difference even after polishing. At present it is hard to measure the thickness from several points of the silicon using the mechanical method which has a large error. Also, the force is not easy to control and it will damage the silicon easily. The application of capacitor non-contact measurement is one of the nondestructive technique [1].

1. FUNDAMENTAL

There are many kinds of measuring circuit for capacitance sensor[1] such as Tightly coupled inductor arm bridge, transformer bridge,double T bridge circuit, differential pulse width modulation circuit, frequency modulation circuit. In this paper, the principle of non contact thickness measurement of capacitance sensor is shown in Figure 1. Two capacitive sensors a and b are spaced at a fixed distance D. At this point the capacitance of a and b is a based static value Ca and Cb. The thickness of the silicon wafer in the D interval is T. It raises the capacitance of Ca and Cb which is processed by the CAV424 capacitance sensor analog circuit and gets an voltage output signal Vb out and Va out.The difference of voltage indicates the difference of capacity Ca and Cb which is related to the thickness T. Since the CAV424 circuit is the differential input and Vc constant current integral form, its linearity is excellent and the resolution can reach 0.1um.

D is a fixed interval. To obtain the thickness T of the silicon wafer:

$$T = D - (a + b) \qquad (1)$$

The a and b in the formula are the distance from the capacitance sensor a or b to the silicon wafer.

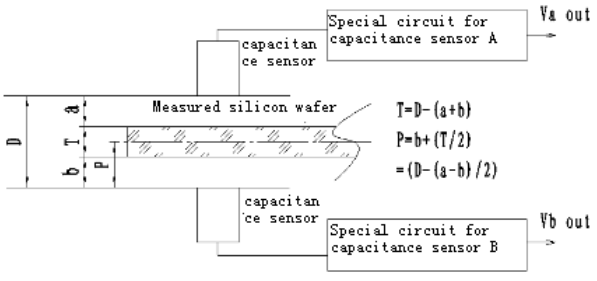

Figure 1

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2. PRINCIPLE OF CAPACITANCE SENSOR

2.1 BRIEF INTRODUCTION OF CAPACITIVE SENSOR

Capacitance sensor is a cylindrical, and the shell is made by su304 stainless steel which is in order to achieve better temperature characteristics of the capacitance plate using titanium alloy material. Annular gap is filled with 0.1mm polyester film, cavity with epoxy resin potting. Capacitance sensor test surfaces are polished to a mirror which is in order to meet the anti-interference requirements of internal wires of each string with a 1K~10K resistance。

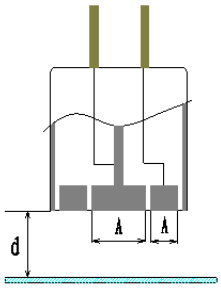

Figure 2 the structure of the single chip capacitance sensor

2.2 CALCULATION METHOD OF INITIAL CAPACITANCE VALUE OF SINGLE CHIP CAPACITANCE SENSOR[2]

$$C = \frac{\varepsilon A}{d} = \frac{\varepsilon_0 \varepsilon_r A}{d} \qquad (2)$$

Among: $\varepsilon_0 = 8.85 \cdot 10^{-12} F \cdot m^{-1}$, $\varepsilon_r =$ Relative dielectric constant,

A= plate area, d= plate distance.

According to the formula, the capacitance C of sensor is changed by the distance, dielectric constant and area. When the dielectric constant and the area of the plate are fixed, the distance is the single value function of capacitance variable C. The characteristic capacitance sensor applications can measure effectively. [9] [10]

3. BRIEF INTRODUCTION OF CAV424 CAPACITANCE SENSOR CIRCUIT [4]

In Figure 3, almost all of the capacitance sensors use differential capacitance method to obtain a linear degree and a larger signal since the capacity of the capacitance sensor varies in a range of pF or up to several hundred Pf. In some applications, the unit of ⊿C is also several pF. In general, a fixed capacitor is chosen as a reference, and the other one is used to measure and amplify the differential signal.

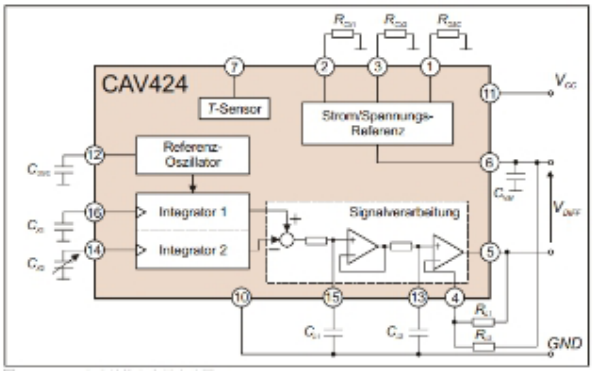

Figure 3 the internal structure of capacitance sensor circuit

3.1 CAPACITANCE INTEGRATOR [4]

Principle of two symmetrical structure built-in capacitor integrator is similar to the reference oscillator above. The difference is that discharge time is half of the charging time. Secondly, the minimum discharge voltage is limited in a built-in fixed voltage vclamp = 1.2 V. (Figure 4).

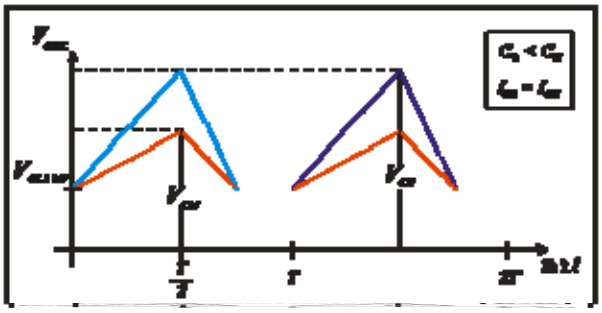

Figure 4 the output voltage of Zeit= two integrator

The capacitive current of ICR integrator and ICM are determined by external resistor RCM, RCR and reference voltage VM：

$$I_{CM} = \frac{V_M}{R_{CM}} \quad \text{and} \quad I_{CR} = \frac{V_M}{R_{CR}} \qquad (3),\ (4)$$

* Formula (3) and (4) do not contain the RCX. At this time the RCX value is zero. To made a good thermal coupling of the resistance, the resistance RCX = 0. Its value can be obtained by calibration software application Kali1_cav424.exc Kali1_cav424.exc and Kali2_cavV424.xls Kali2_cavV424.xls.

Capacitors CM and CR are charged to the maximum value VCM and VCR, which can be calculated by theoretical formula as follows：

$$V_{CM} = \frac{I_{CM}}{2 \cdot f_{OSC} \cdot C_M} + V_{CLAMP} \quad (5)$$

$$V_{CR} = \frac{I_{CR}}{2 \cdot f_{OSC} \cdot C_R} + V_{CLAMP} \quad (6)$$

First, the voltage (VCM) and VCR of two capacitors Cm and Cr are subtracted through the signal processing circuit. Adder-subtractor with the function of rectification also eliminated clamp fixed voltage VCLAMP. A DC voltage signal VTPAS is generated at the output end after filtering.

3.2 THE WORKING PRINCIPLE OF CAV424 [4]

A reference oscillator with adjustable capacitor COSC frequency drives two symmetric structure of integrator and synchronizes in the same time and phase. (Figure 3). The amplitude of two controlled integrator is determined by the result ICR/CR and ICM/CM from current and capacitance value division. CR is used as a reference capacitor and CM is used as a measuring capacitor. The integrator has a high common mode rejection ratio and resolution, so the difference between the two amplitude signal reflects the difference between the two capacitors Cr and Cm.

The voltage difference is filtered by the active power filter and transferred to the DC power source signal. (rectifier effect) And then the signal is sent to the adjustable amplifier to adjust to the desired output voltage value.

If the two current and capacitor division result ICM/CM is same as ICR/CR, the DC voltage signal is zero after rectifying and filtering(Figure 4). If the measured capacitance cm changes Δ CM, the output voltage is proportional to the 1 / Δ CM .

If the second capacitor Cr and cm values are not the same, the output end is a bias value when the Δ CM = 0. It is always superimposed on the DC voltage signal. CAV424 is a multi-purpose and can deal with almost all capacitive sensor signal. It is a complete conversion interface integrated circuit. It also has (relative change of capacitance) signal acquisition, processing and differential voltage output function. CAV424 uses a fixed reference capacitor Cr to get relative change amount Δ CM = CM,max － CM,min of a measured capacitance Cm capacitance.

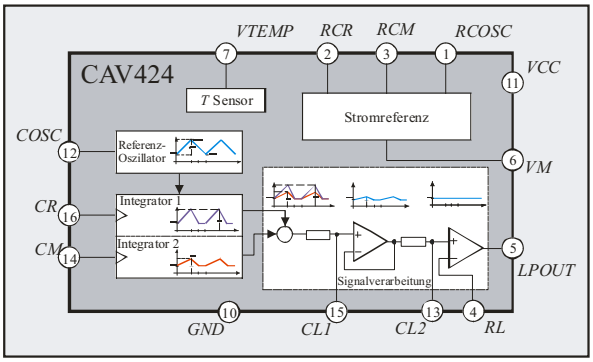

Fig. 5 current block diagram with signal processing

The reference capacitance CR value is set between the 10PF and 1NF with CAV424 design. So that the change of measured capacitance cm Δ CM can be 5% to 100% of based capacitor CR . Differential voltage output can be directly connected to the A / D conversion circuit. A digital calibration circuit system consists of integrated circuit temperature sensor and MCU.

4. APPLICATION OF CAV424

4.1. APPLICATION DESIGN OF CAV424

The circuit is shown in Figure 6. The test circuit is composed of 5 parts. CAV424 is special integrated circuit for capacitive sensor. LPOUT output has a 2.5V DC component which is amplified at the first level by a single chip microcomputer to control the programmable zero point correction circuit and a 2.5V voltage is added at the reverse side so that the output of the first stage is 1V, which is defined as the relative zero point. Programmable zero point correction application

/50K/256 ISL95810 tap digital potentiometer and MCU application STC12C5604AD use the 10 bit AD converter in the circuit to monitor and adjust the zero point of the first stage DC amplifier.The first stage of the DC amplifier is fixed, and the second stage is a variable gain amplifier which is controlled by MCU /50K/256 ISL95810 tap digital potentiometer to achieve gain adjustable.This adjustment is allowed to operate in standard sample calibration.

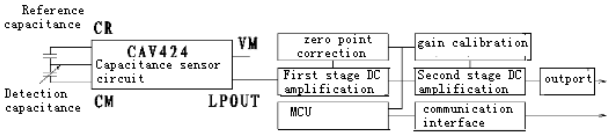

Figure 6 application circuit diagram

Application circuit CAV424 in silicon wafer thickness testing system is used in pair. The test system can be a point or several points of the form of architecture. Start and idle status of test points are controlled by a PC operating system software in real time. The second stage DC amplifier output is the final analog output for the modulus of PC-ADC conversion to calculate the thickness of the test point [6] [7] [8] [11]。CAV424 application schematic diagram is shown in Figure 7; PCB application CAV424 diagram shown in Figure 6.

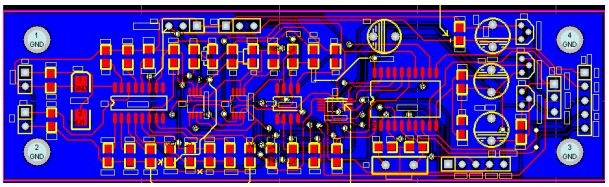

Figure 7 CAV424 application PCB diagram

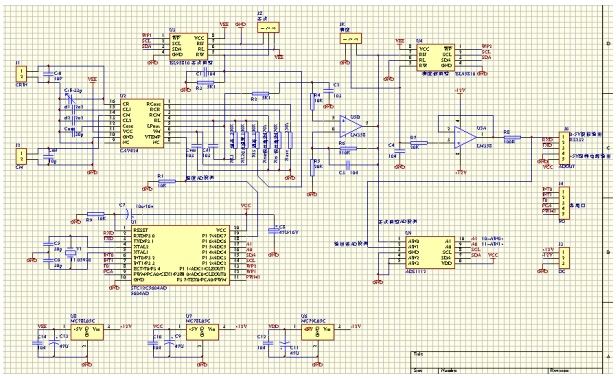

Figure 8 Schematic diagram of CAV424 application

4.2. CAV424 LINEAR RANGE AND TEST DATA ANALYSIS

CAV424 working voltage is 5V. The test sensor face to face coaxial installation distance is 4mm. Designed test wafer thickness range is 0 ~ 1 mm. CAV424 output voltage is 2.5V~4V. The absolute value of once signal voltage is 1.5V. After zero point correction, the first stage amplifier gain is Vout1=lpout(1+Rf1/Rb1)=1.5V(1+1)=3V and the second gain stage is depend on the IPC-9112ADC sampling card benchmark 10V, which is 1mm output voltage maximum 10V, and the gain is Vout2=10/3=3.33333 times.

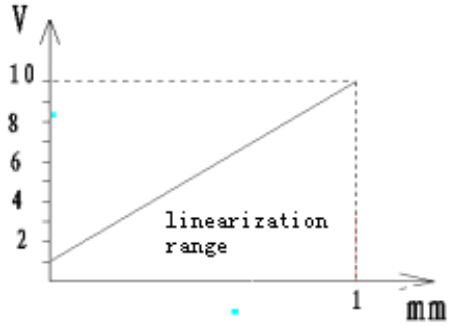

Figure 9 linear regions of test data

Figure 9 shows the test data linear region which contains an important zero point concept.

The output of the two capacitance sensors in the absence of silicon wafer should be 0V and the pitch size is D=4mm. Since the silicon chip's intervention has changed the dielectric constant to increase the capacity of the sensor, at this time, the initial value of zero adjustment of its critical values are 1V.In the 1/2 D as the interface line, when a sensor and the silicon wafer surface is 1mm, the output of the second amplifier is adjusted to 10V, The actual thickness of the linear variable ranges 0~1mm, and the voltage variable ranges 1~10V, and the resolution is 1mm /9=0.11111 um/V.In the D interval 0~1mm is Va, a is 1~10V; B is 0~1mm, Vb is 1~10V; VD=Va+Vb=18V. The measured data are shown in Table 1.

Table -1 test data table of two kinds of silicon wafers

No	Standard thickness	Measured thickness	Measured voltage	Measured thickness	error
1	0.242 (mm)	2.178 (V)	0.011 (V)	0.243 (mm)	0.001(mm)
2	0.247	1.223	1.009	0.248	0.001
3	0.245	2.205	0.013	0.246	0.001
4	0.603	4.427	1.003	0.603	0
5	0.606	5.454	0.007	0.607	0.001
6	0.606	4.451	1.010	0.607	0.001

According to the formula（1）

T = D – (a + b). Converted to voltage representation algorithm：

Thickness

T(mm)=VD-(Va+Vb)=18v-((9V-Va+(9v-Vb))*0.1111

T(mm)=18V-((9v(1-Va)+(1-Vb))*0.1111 (7)

Example: according to table 1 serial number 1 in the input data type（7）

T(mm)=–((9V(1-2.178)+(1-0.011)*0.1111=

(18-15.811)*0.1111=2.189*0.1111=0.24319mm。

After the decimal point is retained 3, the thickness of the test is 0.243mm, which is 0.001mm larger than the sample.

According to formula (7) test results show that silicon in the D timeline does not affect the accuracy of the test data. Therefore, the method based on CAV424 capacitance sensor circuit of non-contact wafer thickness measurement has high technical feasibility and practical value.

5. Conclusion

After practical application, CAV424 capacitance sensor application specific integrated circuit of non-contact wafer thickness testing system design and test device structure has high precision, simple circuit, convenient adjustment, and extremely high performance price ratio. The design has been applied in non-contact thickness measurement function of multifunctional solar silicon wafer tester.

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