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# Gate Engineering in SOI LDMOS for Device Reliability

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**Abstract.** A linearly graded doping drift region with step gate structure, used for improvement of reduced surface field (RESURF) SOI LDMOS transistor performance has been simulated with 0.35µm technology in this paper. The proposed device has one poly gate and double metal gate arranged in a stepped manner, from channel to drift region. The first gate uses n+ poly (near source) where as other two gates of aluminium. The first gate with thin gate oxide has good control over the channel charge. The third gate with thick gate oxide at drift region reduce gate to drain capacitance. The arrangement of second and third gates in a stepped manner in drift region spreads the electric field uniformly. Using two dimensional device simulations, the proposed SOI LDMOS is compared with conventional structure and the extended metal structure. We demonstrate that the proposed device exhibits significant enhancement in linearity, breakdown voltage, on-resistance and HCI. Double metal gate reduces the impact ionization area which helps to improve the Hot Carrier Injection effect.

## 1 Introduction

Laterally double diffused metal oxide semi-conductor (LDMOS) on SOI substrate is a promising technology for smart power transistors. Having applications in automotive, display drivers, digital audio and power management, power switching devices etc. In the recent past, developing high voltage SOI LDMOS has gained importance due to possibility of its integration with low power devices and heterogeneous microsystem.

Also in SOI LDMOS the kink appearing in the output characteristics. Though the kink can be eliminated by reducing the drift region doping concentration, [1] the increased drift region resistance degrades the other device parameter. Therefore, the motivation of this work is to explore structural modification in SOI LDMOS to enhance its high voltage capabilities and ruggedness of the device.

The SOI technology is interesting for three primary reasons. The buried oxide in the SOI structure reduces capacitive coupling to the substrate, which improves power efficiency. The SOI buried oxide also provide improved isolation between adjacent circuits, making attractive for highly integrated power amplifiers in which substrate cross talks is a concern. A third advantage is that it allows for the use of high resistivity substrates that enable the fabrication of low loss on-chip inductors.

## 2 Device structure

Fig. 1 shows the cross-section of our SOI double metal gate with P-top LDMOS device. The device is characterised by the double metal gate in the drift region. The first gate uses n+ poly as the gate material and the other two gates uses aluminium as the gate material. The first gate having the higher work function material (n+ poly) tries to increase the threshold voltage, but the thinner first gate oxide reduces it. Thus the design of step gate LDMOS is done in such a way that the combination of thinner and higher work function material results in the same threshold voltage as that of the conventional device.

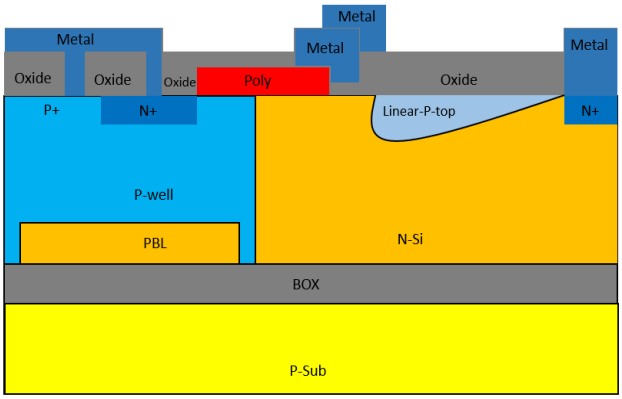


**Figure. 1** Cross-section of step gate SOI LDMOS with linear P-top

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We developed a new innovative n-channel LDMOS device with P-top in the drift region. P-top in the drift region helps to achieves better RESURF condition, contributes to uniform electric field. [2] [5]

Table 1. Off-state characteristics

| | BVDs(V) | Ron(mΩmm$^2$) | Vth(V) |
|---|---|---|---|
| Conventional structure | 92.3 | 133 | 1.85 |
| Single Metal Structure | 100.2 | 119 | 1.5 |
| Double Metal Structure | 98.2 | 119 | 1.5 |

## 3 Kirk Effect

For lateral high voltage devices at high current density, the moving carriers influence the depleted charge, which results in high electric field near N/N+ junction. This is called Kirk effect. In the on-state significant amount of negative charge adds to the positive space charge of the N-type drift region.

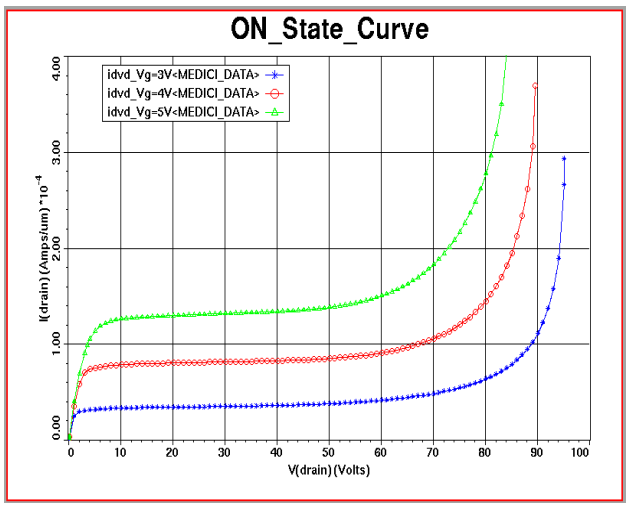


**Figure 2.** IV curve for double metal proposed SOI LDMOS device structure

It leads to a shift of the potential lines towards the drain. For application, the effect means the use of a longer drift region or less current per gate width.

Several methods have been proposed to alleviate Kirk effect, adding an $N^-$ buffer region, whose concentration is higher than the drift region while lighter than the drift region, has been well-known. A double RESURF technology was put forward to improve SOA. [2]

## 4 Hot Carrier Effect

As the electric field increases, electrons and holes traveling in the channel and drift region may gain sufficient kinetic energy to be overcome a potential barrier necessary to the SiO2 interface, and cause in the SiO2 interface charge distribution. This defines the well-known hot carrier effects (HCI), which is one of the major failure mechanisms affecting long term reliability. In the case of LDMOS applied with high voltage to the gate and drain HCI severe limitation to long term (LT-SOA). [2]

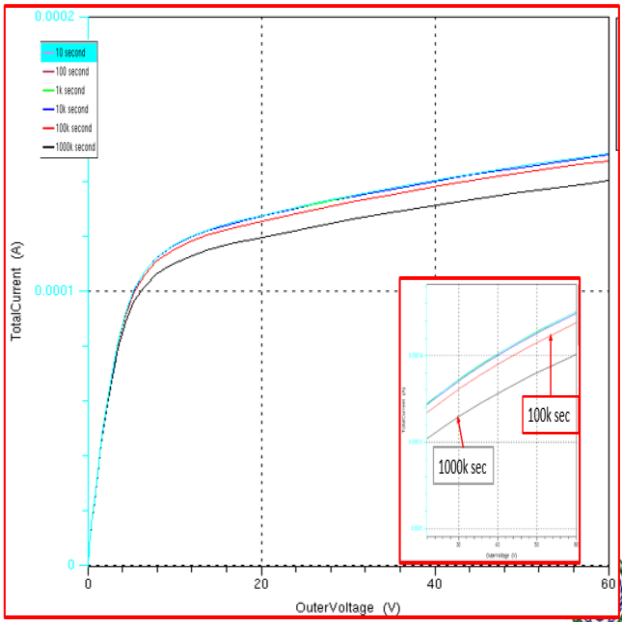


**Figure 3.** $Id_{sat}$ Conventional Structure compasion for 10k sec, 100k sec, 1000k sec

As a matter of fact, HCI are induced by high electric field consequently, any action devoted to reduce the peak/plateau of the electric field in the channel and the drift region can improve the ruggedness of LDMOS and increase the corresponding LT-SOA. [2]

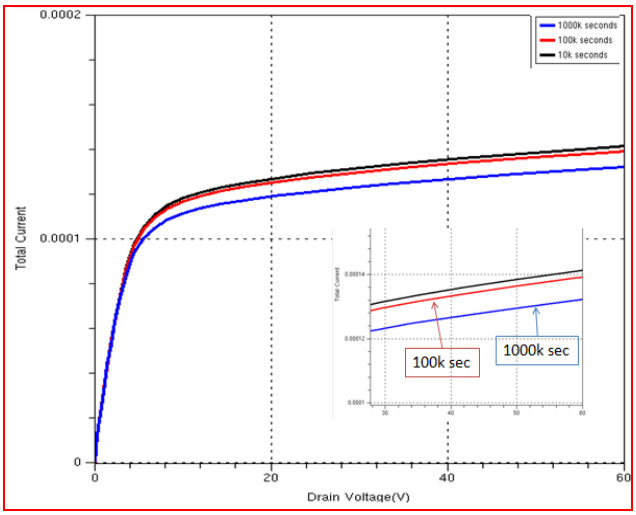


**Figure 4.** $Id_{sat}$ Double Metal Structure compasion for 10k sec, 100k sec, 1000k sec

Table 2. $Id_{sat}$ percentage change

| Stress time(sec) | % shift Conventional Structure | % shift Double Metal Structure |
|---|---|---|
| 1E4 sec | 0.29 % | 0.20% |
| 1E5 sec | 1.78 % | 1.75% |
| 1E6 sec | 6.5 % | 5.9% |

## 5 Design Issues

A LDMOS drift region is the most important and complex part. This part has significant influence on breakdown voltage, on resistance, power consumption, device stability and reliability of SOI LDMOS. [6] Each parameter in the design of drift region will have an impact on device performance, and different process parameter has mutual influence between them. Higher breakdown voltage requires lightly doped, thick and long drift region, while low on resistance require heavily doped thin and short drift region. So the design of SOI LDMOS needs to balance between drift region doping concentration and length, maintaining certain breakdown voltage of the device and achieve the least on resistance. [7]

The main principle of the extended P-top region is to reduce the parasitic BJT effect. The hole current generated due to impact-ionization is now collected through n+ and P-top junction instead of an n+ and p-body.

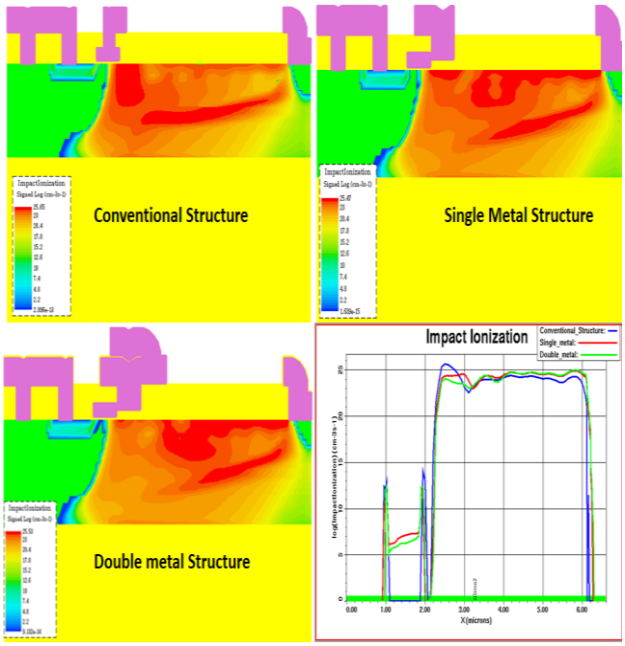


**Figure 5.** Impact Ionization area comparison in three different structure.

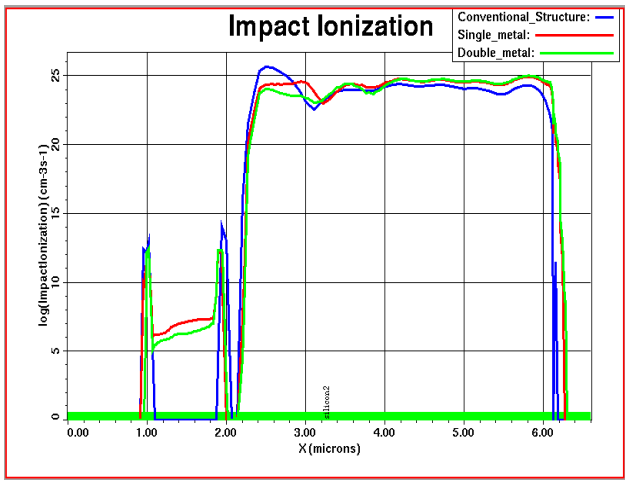


**Figure 6.** Impact Ionization curve comparison in three different structure.

### *5.1 Electric field distribution*

The stepped gate structure in the drift region has three gate sections arranged with increasing gate oxide thickness from the channel side to the drain side. [3] The stepped gate structure leads to uniform electric field distribution, reduced gate-drain capacitance and facilitates the use of increased drift region doping simultaneously. [4] The gate overlap length and the stepped oxide thickness for both the devices in our simulation are designed for maximum breakdown voltage and minimum on-resistance.

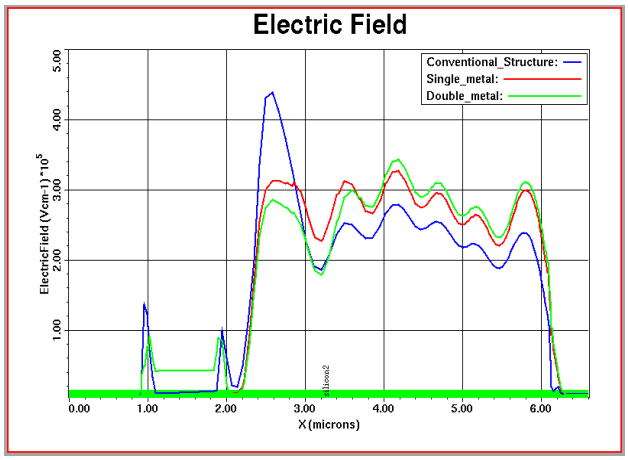


**Figure 7.** Electric field distribution in three different device structures.

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