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Analysis of Kirk effect of an innovated high side Side-Isolated N-LDMOS device

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Abstract. An ESOA of LDMOS device is very critical for power device performance. Kirk effect is the one of the major problem which leads to poor ESOA performance. The cause of the problem mainly due to the high beta value of parasitic NPN transistor in the p-body. In this study, we proposed a new 3D high side Side-Isolated N-Channel LDMOS which we have obtained not only benchmark Ron and breakdown performance, but also better ESOA without Kirk effect. We have compared the analysis of Kirk effect between the new device and the conventional N-LDMOS structure with LATID technique for the formation of the p-body of both device structures.

1 INTRODUCTION

LDMOS transistors are widely used in smart power technologies; Applications are in display drivers, digital audio and power management, Power switching devices etc. Because of its low channel resistance, favourable increase in Transconductance, compatibility and efficient use of silicon area of industrial, consumer electronics and automotive electronic control systems. It requires good robustness and ESOA performance against ESD damage, high temperature operation. One of the problems for On-state I-V curves is Kirk effect and we optimized beta of the parasitic NPN transistor for reducing the Kirk effect [3].

The current gain drops at high collector currents due to yet another mechanism known as the Kirk effect. Kirk effect is an important phenomenon in bipolar junction transistors at the high current condition in Figure1, especially for the HV devices with light-doped concentration, it is necessary to take the Kirk effect into consideration because most of ESD protections operate in the parasitic BJT mode. Kirk effect leads to the base extension and the peak electric field migration which greatly affect the device characteristics. Besides, the peak electric field shifted in the highly doped collector region can results in higher impact ionization rates, which promote the increase of avalanched electron-hole pairs [1] [2].

In this study we studied Tilt angle implantation and we found tilt 30 ° is the best solution for impact ionization performance. The optimization of high side lateral double-diffused Metal Oxide Semiconductor (LDMOS) With Side-Isolated 3D device replaced for the conventional 2D RESURF LDMOS device. Because, the conventional 2D RESURF LDMOS device is always suspected ably as it has Kirk effect and high leakage current problems. These will cause poor reliability and also robustness problems in the devices. So, we studied LATID process and heavier P-body doping concentration.

We found optimization the process and this design is implemented by conventional 2D RESURF LDMOS device and 3D high side Side-Isolated LDMOS structures. We found better choices for tilt 30 ° to achieve good Breakdown voltage, Low On-State Resistance and it indicates a good choice for Impact ionization.

In this work, we developed a new innovated high side Side-Isolation N-channel LDMOS 3D device on both front and back edges of the extended drift region. First, we developed the conventional 2D RESURF LDMOS and when we analyzed the electrical characteristics we noticed the high leakage current and Kirk effect problems in On-state characteristics. We innovate that one of the best solution is replaced by the 3D high side Side-Isolated device with thermo-oxide deposition and the leakage current is substantially decreased and Kirk effect problems also solved as compared to the conventional 2D RESURF LDMOS device. We demonstrated these phenomena's by using N-LDMOS device we developed by using Sentaurus simulation (3D) in Figure 2.

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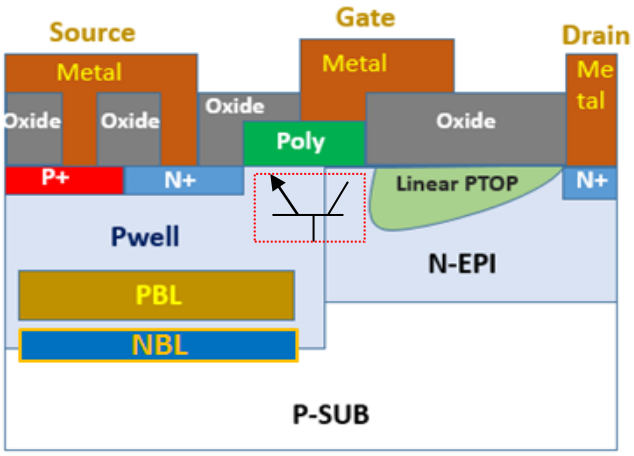


Figure 1. The High side device Under study using N-LDMOS with linear p-top. The parasitic NPN transistor is shown.

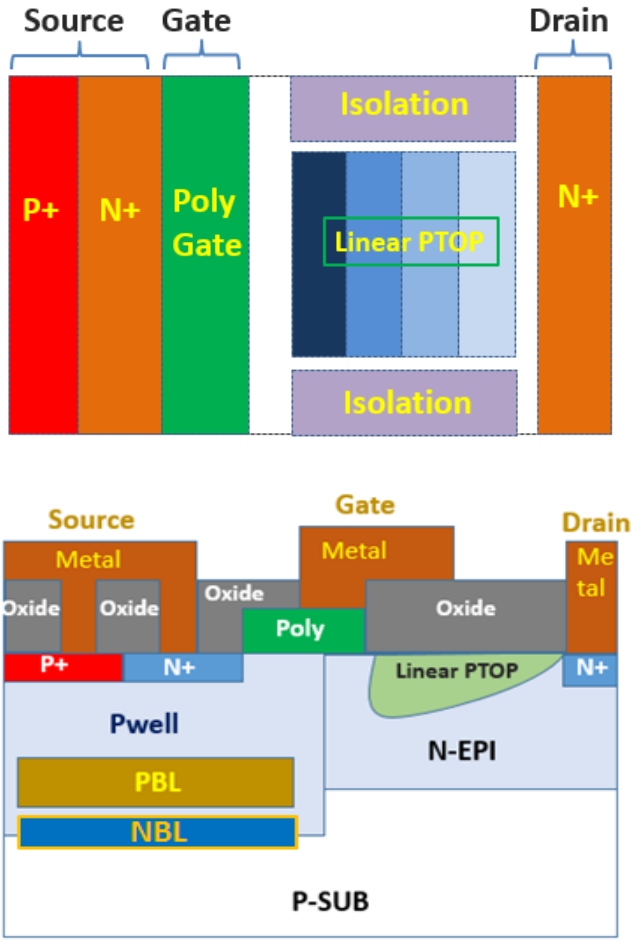


Figure 2. Schematic of 3D high side Side-Isolated N-LDMOS Structure (3D) (a) top view (b) cross section.

2 SIMULATION RESULTS AND DISCUSSION

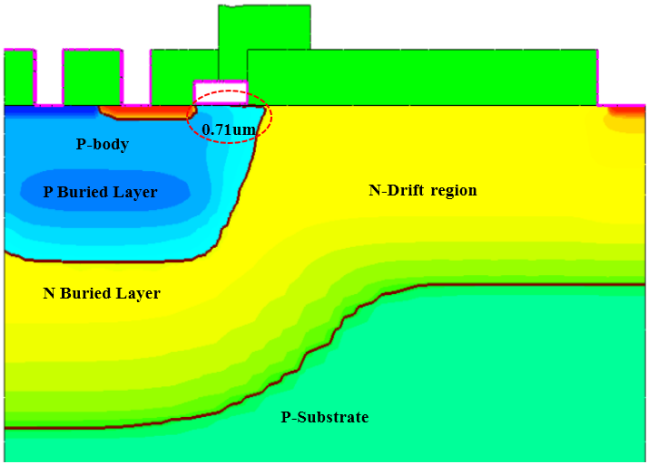
We demonstrate the leakage current and Kirk effect problems in conventional 2D RESURF LDMOS structure and thereby affecting very important ESOA performance of the device. So, we designed 3D high side Side-Isolated techniques to reduce the beta of the parasitic NPN transistor thereby to avoid the Kirk effect and reduce the leakage current. With our new 3D High side Side-Isolation structure had 0.71um p-body width and conventional 2D structure had 0.57um p-body width. It indicates longer channel width is used to reduce the beta of the parasitic NPN transistor, In Figure 3 as we show the comparisons of the channel width between 3D high side Side-Isolated and conventional RESURF LDMOS devices.

We found the heavier p - body doping concentration average ($10^{\wedge 17}$ atoms/cm-3) in 3D side isolation structure and conventional 2D isolation device found less average p-body doping concentrations ($10^{\wedge 16}$ atoms/cm-3) as shown in Figure 4 and Figure 5. We simulated the on-state curves to analysis the Kirk effectively as we can see in Figure 6 and Figure 7.

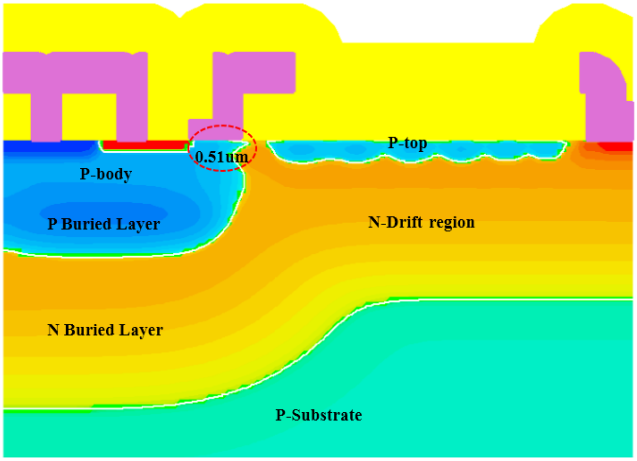
The heavier doping concentration and longer channel make the Kirk minimize. We optimize the LATID process with different tilt angle implantation(7 °, 30 °, 45 ° and 60 °) and we found 7° showing the severe Kirk effect and Tilt 30° also found the best solution for Kirk effect problems in 3D high side Side-Isolated device. [4][5]

The 3D structure is showing higher p-body concentration and longer channel length as compared to the conventional 2D RESURF LDMOS device. The comparison of Off-state leakage current between 3D high side Side-Isolated N-LDMOS and conventional 2D RESURF LDMOS device at room temperature, there we can see the leakage current in a 3D Side-Isolated device is substantially reduced as compared with conventional 2D structure and it is around 10 times lesser than conventional 2D RESURF LDMOS device. The electrical characteristics comparison between 3D high side Side-Isolation device and conventional 2D RESURF LDMOS device shown in Table 1.

The Kirk is one of the most consider as N-LDMOS power device. We found LATID is one of the solutions for 2D.However the Kirk is disappearing in new innovated 3D high side Side-Isolated N-LDMOS structure because of side isolation techniques. Hence side isolation technique is one of the best solutions to solve Kirk effect problems and enhance the leakage current in smart power devices.



(a)



(b)

Figure 3. Device comparison between (a) 3D high side Side-Isolated with p-body and (b) Conventional 2D RESURF LDMOS Structure.

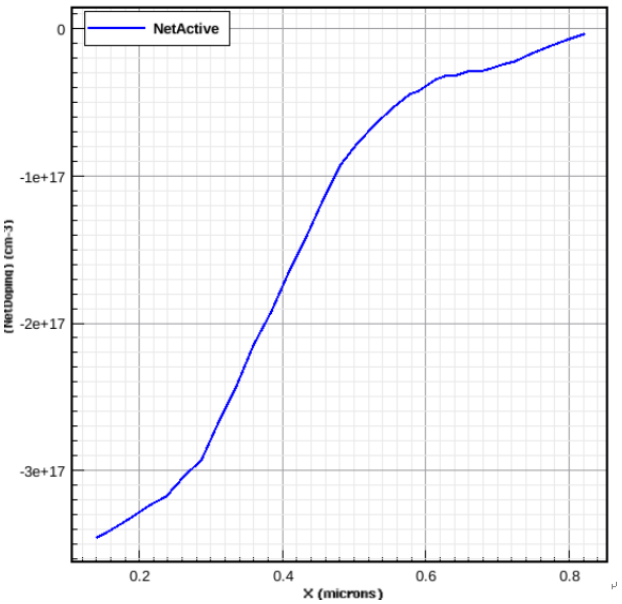


Figure 4. P-body doping concentration (atoms/cm-3) in 3D High Side Side-Isolated device.

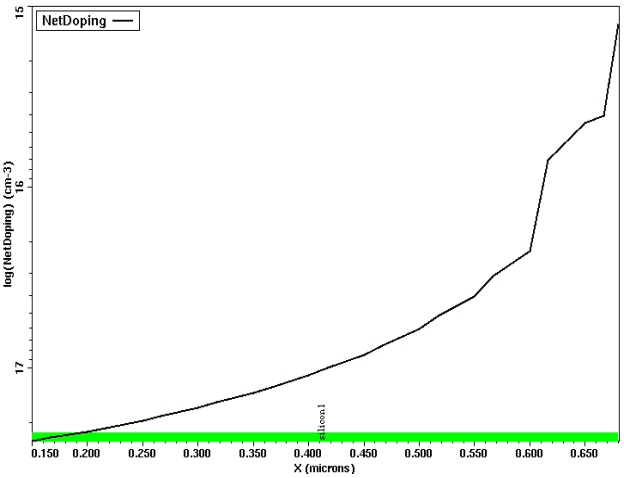
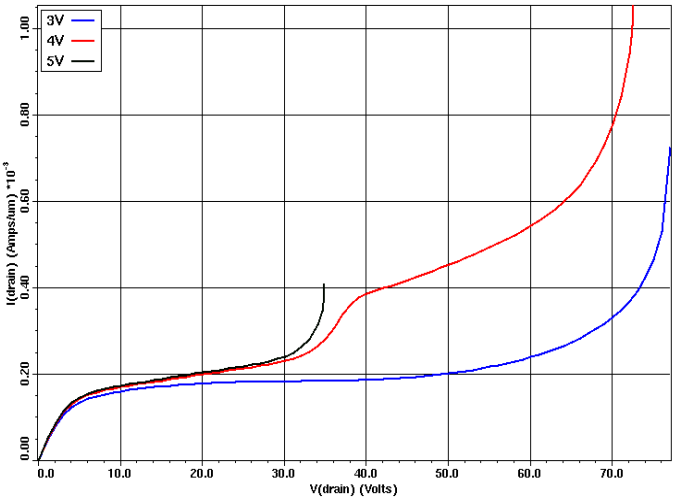
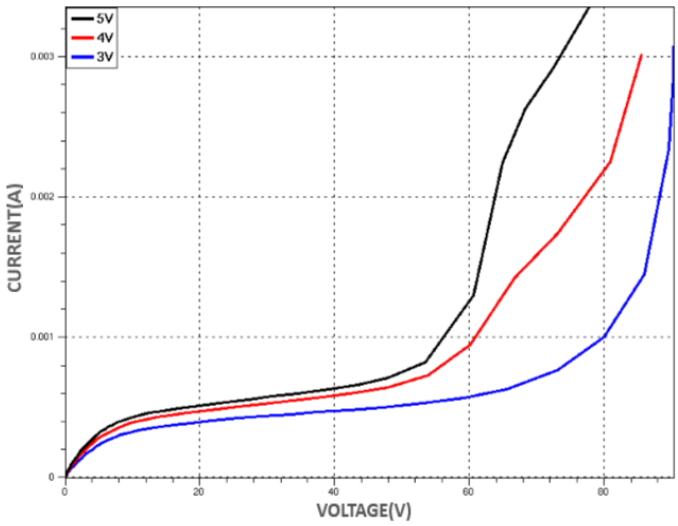


Figure 5. P-body doping concentration Conventional 2D RESURF LDMOS structure.



(a)



(b)

Figure 6. N-channel LDMOS On-state I-V curves comparison between 3D high side Side-Isolated with linear p-top and Conventional 2D RESURF LDMOS device.

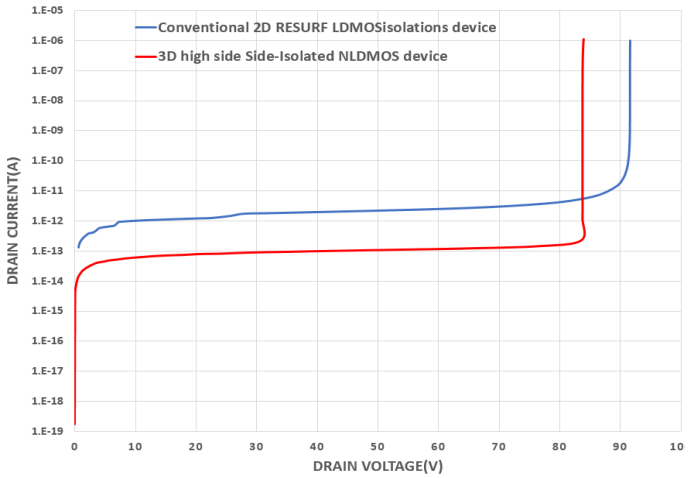


Figure 7. Plot of Id (A) verses Vd (V) showing the leakage current comparison between 3D high side Side-Isolated device and conventional 2D RESURF LDMOS device.

Table 1. Electrical characteristics comparison between 3D high side Side-Isolated N-LDMOS and 2D conventional RESURF LDMOS device.

Electrical Characteristics	Conventional 2D RESURF LDMOS device	3D high side Side-Isolated N-LDMOS device
Lateral BVD(V) at 1e-6	91.6	83.9
Vertical BVD(V) at 1e-6	482.3	109.4
Ron (mohm-mm2)	90	45.1
P-Body width(um)	0.51	0.71
BVD(V) for vg=3v	77	90.3
BVD(V) for vg=4v	72.5	85.6
BVD(V) for vg=5v	35	77.9
Kirk Effect	Yes	No

3 CONCLUSION

We have studied 3D high side Sided-Isolated N-LDMOS and conventional 2D RESURF LDMOS device and we found a Kirk effect in On-State I-V curves and this Kirk effect depends on P-body doping concentration and channel length and these interns depend on LATID. We proved this new 3D high side Side-Isolated structure can increase p-body concentration and channel as well. This device design will solve Kirk effect problems. So it shows better ESOA performance and also improved Off-state leakage current. It will boost UIS performance as well. Even the process and timing same, but the structure only different. It is one of the better solutions for smart power applications.

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