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Design of the adaptive log-domain low-pass filter

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Abstract. This paper presents the structure and realization method of the current-controlled adaptive low-pass filter which based on the design of LC ladder network. After amplifying, amplitude limiting and shaping, the input voltage signal was converted into frequency signal. Then by the broadband frequency-current conversion circuit it was converted into current signal which has a linear relationship with input frequency. The current signal was as the bias current to adjust the cut-off frequency of the log-domain low-pass filter. So that frequency of the filter can automatically track the input signal frequency. In this paper, the design principle was introduced in detail, the design formulas were derived and the circuit of adaptive second order log-domain low-pass filter was given. The filter can realize the scope of the cut-off frequency up to 30MHz. The tracking range for the input frequency is from 1MHz to 30MHz. The simulation results show the effectiveness of design method.

1 Introduction

Filter has a wide range of applications in the fields of the signal processing, the data transmission and interference suppression [1-2]. Especially, adaptive filter plays an important role in the field of the adaptive signal processing and has the distinctive features of filter frequency following the change of input signal frequency automatically [3-4]. When signal processing, the test signal will inevitably be doped with noise. The filter which has fixed frequency can only realize signal filtering within a small frequency range. However, the adaptive filter can change the filter frequency according to the change of the signal, it is good to suppress the noise, and it has good filtering performance.

At present, there are many kinds of methods to implement analog adaptive filter. The first is the state variable method which can realize low-pass, high-pass, band-pass, band-stop and all-pass filter simultaneously, but the design and debug are troublesome and difficult to control, and besides the components are discrete and the non-linear effects are large [5-7]. The second method is the voltage-controlled method. Using this method, the offset voltage and drift will directly affect the stability of the low frequency [8-9]. The third method is using existing integrated filter chip. This method does not require to know the signal frequency in advance, the stability is better and cut-off or central frequency is controllable, but there are some large circuit noise and signal aliasing problems in the course of the use, even through clock frequency or pin programming is difficult to achieve the filter cut-off frequency or central frequency continuous change [10-12]. If the signal frequency changes in a wide range, the above three tracking methods are unable to achieve the fast tracking of the signal frequency. Log-domain filter is a current mode circuit in the true sense, which has been widely used in electronic systems by virtue of the advantages of power supply voltage, low power consumption, wide dynamic range, high frequency, wide tuning range and good linearity, and improves signal processing accuracy further [13-14]. This paper presents a design method of analog adaptive filter which use high-performance broadband frequency current converter (F/I) circuit, combined with the log-domain filter with transistors as the core elements to achieve the analog filter whose cut-off frequency can fast adapt the change of processed signal frequency automatically. The design of log-domain adaptive filter compared to other adaptive filters, it has the advantages of a low power consumption, high filtering frequency, wide dynamic range and low distortion. It can be applied in these cases: a wide range of signal frequency changing, a high-speed of the filtering, and filter frequency is not fixed.

2 Working principle

The principle diagram of the adaptive log-domain low-pass filter is shown in figure 1. The input voltage signal V_i gets through the amplifier to output voltage signal V_x .Then the voltage signal V_x is divided into two paths, the first will get through the limiting circuit and over-voltage comparison circuit which MAX903 is the core component to be shaped to send signal into the broadband F/I circuit, and then the bias current signal I_B output from

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F/I circuit is sent to the log-domain low-pass filter to control the cut-off frequency. The other one will get through the voltage current conversion (V/I) circuit to send current signal i_i into the logarithmic compression circuit to be pre-processed, and then the logarithmic compression circuit output current signal i is as the input signal of the log-domain low-pass filter.

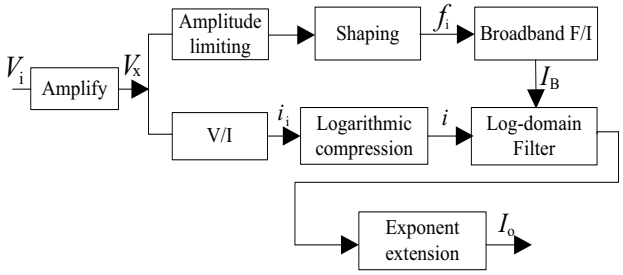

Figure 1. The diagram of adaptive log-domain low-pass filter.

2.1 Broadband frequency current conversion(F/I) circuit

The principle diagram of the broadband F/I circuit is shown in figure 2, which consists of the main control circuit, the frequency division circuit, the F/I circuit and the current amplification circuit. Since the chip AD650 which in the F/I circuit maximum switching frequency is 1MHz, so the high frequency signal to be processed first need dividing frequency after shaping. The principle of realizing broadband F/I circuit is the processed frequency signal f_i after shaping first gets through 400 frequency division circuit to send signal f_{i1} into main control circuit in which control chip is 89s52. Main control circuit calculates and compares parameters in its internal to choose the appropriate frequency division multiple, and then controls frequency division circuit to re-divide frequency for the signal after shaping. Meanwhile, it controls current amplification circuit to generate the corresponding magnification. The re-divided frequency signal gets through F/I circuit to convert frequency signal to current signal, and it will go into current amplification circuit. The I_B is output current of broadband F/I circuit.

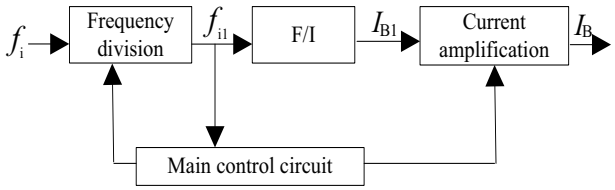

Figure 2. The diagram of broadband frequency-current conversion circuit.

The F/I of figure 2 is shown in figure 3, it converts input pulse signal into current signal. Input pulse frequency has a linear relationship with output current value, so it is possible to measure the input pulse frequency indirectly by measuring the output current value. F/I circuit is composed of the frequency voltage (F/V) conversion chip AD650, operational amplifier OP37 and a small amount of resistors and capacitors.

In figure 3, the input pulse f_{i1} through the coupling capacitor C_1 to be sent into AD650 internal comparator, when its potential is low to the comparator reference potential (-0.6V), internal current switch to end of integral capacitor C_{INT} and charge for it. When the leakage current on R_4 and the charging current on C_{INT} is equal, the voltage on the C_{INT} is stability. The output voltage U_i of pin 1 is proportional to the input frequency f_{i1}, that is

$$U_i = t_{OS} \times R_{INT} \times f_{i1} = (C_{OS} \times 6.8 \times 10^3 + 3.0 \times 10^{-7}) \times R_4 \times f_{i1} \quad (1)$$

Then input U_i into the subsequent V/I circuit in which operational amplifier OP37 is as the core component.

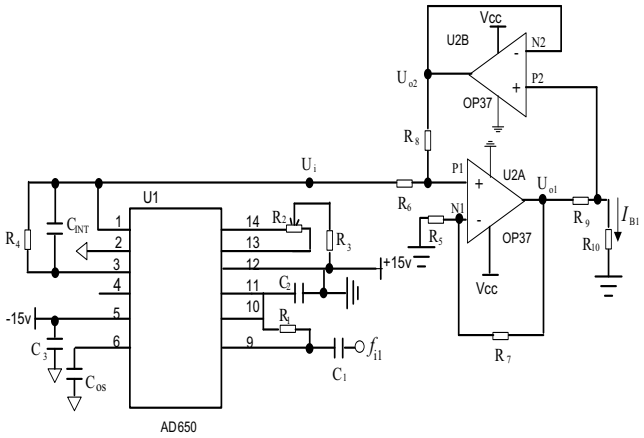

Figure 3. F/I circuit.

For the op-amp U2A and U2B, it can obtain

$$U_{O1} = (R_7 / R_5 + 1) U_{P1} \quad (2)$$

$$U_{P1} = U_i R_8 / (R_6 + R_8) + U_{P2} R_6 / (R_6 + R_8) \quad (3)$$

The voltage on R_9 is $U_{R9} = U_{o1} - U_{P2}$, the eqution (2) and (3) are substituted into U_{R9} , it can deduce

$$U_{R_9} = (1 + R_7 / R_5)[U_i R_8 / (R_6 + R_8) + U_{P2} R_6 / (R_6 + R_8)] - U_{P2} \quad (4)$$

When taking $R_5 = R_6 = R_7 = R_8 = 47$K, then $U_{R9} = U_i$, it can deduce

$$I_{B1} = U_{R_9} / R_9 = U_i / R_9 \quad (5)$$

The eqution (1) is substituted into eqution (5), and due to $I_B = mI_{B1}$, $f_i = mf_{i1}$, in figure 2, m=400. it can deduce

$$I_B = [(C_{OS} \times 6.8 \times 10^3 + 3.0 \times 10^{-7}) \times R_4 / R_9] \times f_i \quad (6)$$

It can be seen from eqution (6) the output current will change linearly with input frequency as long as adjusting the value of resistors and capacitors reasonably.

2.2 Log-domain filter

There is a strict logarithmic relationship between the input voltage and output current of the transistor $v_{BE} = V_T \ln(I_C/I_S)$. According to the characteristics, people use

transistors as core component to build the log-domain filter circuit, so as to realize linear circuits by using nonlinear components. Compared with the traditional filter, log-domain filter has advantages in the frequency characteristic, processing speed, and signal bandwidth. It can meet the requirements of wide tuning range and good linearity when the modern electronic products work under the condition of low voltage.

Log-domain filter is composed of logarithmic compression circuit, the state space of nonlinear filter circuit and the exponent extension circuit, its composition block diagram is shown in figure 4. Input current signal gets through the logarithmic compression circuit to be processed and converted into a logarithmic domain. Weak signals are amplified to a much greater than the noise signal level, and strong signals are compressed to less than distortion level, thus preventing signal distortion and expanding the dynamic range of the circuit. After logarithmic compression circuit processing, the output voltage signal is processed by the state space nonlinear filtering circuit realized by bipolar transistors, so can make the system achieve a particular filtering function. The signal after filtering is decompressed by the exponent extension circuit and converted into a linear domain. Namely process signal nonlinearly again, the weak signal is attenuated, and the strong signal is amplified, so as to restore the proportion of the original signal, making the system into a linear system.

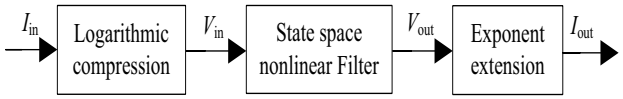

Figure 4. The diagram of log-domain filter.

3 Design of adaptive second-order log-domain low-pass filter

The proposed adaptive second-order log-domain low-pass filter is designed based on LC ladder network, mainly using the broadband F/I circuit, V/I circuit, the transistors, and a small amount of resistors and capacitors. The low-pass LC ladder prototype circuit is shown in figure 5.

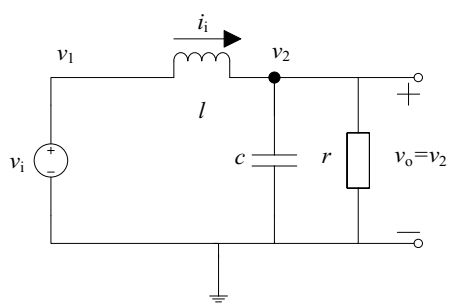

Figure 5. Prototype circuit of low-pass LC ladder.

The transfer function of the LC ladder prototype circuit is:

$$H(\mathrm{s}) = V_{\mathrm{o}}(\mathrm{s}) / V_{\mathrm{i}}(\mathrm{s}) = [1/(lc)] / [s^2 + s/(rc) + 1/(lc)] \quad (7)$$

And the transfer function of the standard low-pass filter is:

$$H(\mathrm{s}) = K\omega_0^{\ 2} / (s^2 + s\omega_0 / Q + \omega_0^{\ 2}) \quad (8)$$

Comparing the eqution (7) with (8), it can deduce cut-off frequency ω_0 of LC ladder filter:

$$\omega_0 = 1/\sqrt{lc} \quad (9)$$

quality factor $Q = r\sqrt{c/l}$ and dc gain K=1.

The log-domain filter corresponding to the LC ladder filter is shown in figure 6, it is made up of transistors and a small amount of capacitors.

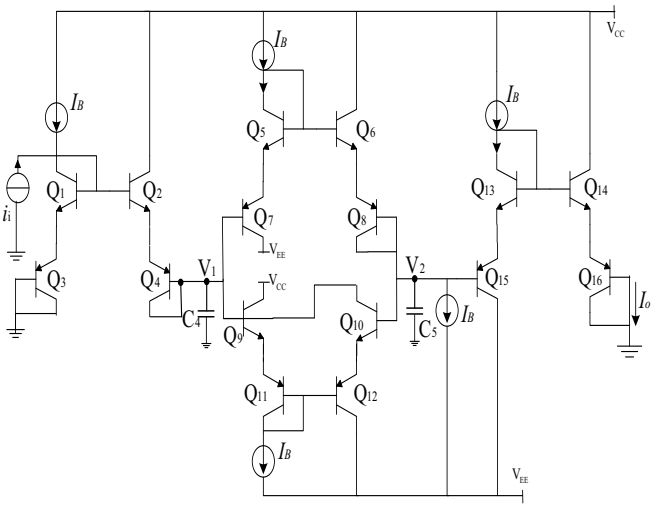

Figure 6. The circuit of log-domain filter.

The in-phase integrator which is composed by transistors Q1-Q4 and capacitor C_4 implement in-phase integral operation and logarithmic operation for the input current i_i. Transistors Q9-Q12 and capacitor C_5 realize inverse integral operation to voltage V_2. Transistors Q13-Q16 controlled by the bias current compose exponent extension circuit. I_B is produced by figure 2, which is as the bias current control end of the log-domain filter.

According to Kirchhoff's law for capacitor C_4 node, we can obtain:

$$C_4 dV_1/dt = i_i e^{-V_1/2V_T} + I_B e^{-V_1/2V_T} - I_B e^{(V_2-V_1)/2V_T} \quad (10)$$

On both ends of eqution (10) multiplied by $e^{V_1/2V_T}$ at the same time and adjust the order, it can deduce

$$2C_4 V_T / I_B \cdot [d/dt(I_B e^{V_1/2V_T} - I_B)] = i_i - I_B e^{V_2/2V_T} + I_B \quad (11)$$

In addition, the LOG and EXP mapping function is:

$$\mathrm{LOG}(x) = 2V_T \ln[(I_B + x)/I_B] \quad \mathrm{EXP}(x) = I_B e^{x/2V_T} - I_B \quad (12)$$

The eqution (12) is substituted into eqution (11), it can deduce

$$\mathrm{EXP}(V_1) = I_B / (2V_T C_4) \cdot \int [i_i - \mathrm{EXP}(V_2) i_i] dt \quad (13)$$

From figure 5, we can obtain:

$$\mathrm{EXP}(V_1)=1/l\cdot\int[i_i-\mathrm{EXP}(V_2)]dt \tag{14}$$

Comparing the eqution (13) with eqution (14), it can deduce

$$l=2V_TC_4/I_B \tag{15}$$

By the same token, writing KCL equation of capacitor C_5 node and using the LOG and EXP mapping function, we can get:

$$\mathrm{EXP}(V_2)=I_B/(2V_TC_5)\cdot\int[\mathrm{EXP}(V_1)-\mathrm{EXP}(V_2)]dt \tag{16}$$

From figure 5, we can obtain:

$$\mathrm{EXP}(V_2)=1/c\cdot\int[\mathrm{EXP}(V_1)-1/r\mathrm{EXP}(V_2)]dt \tag{17}$$

When taking r = 1Ω, comparing the eqution (16) with eqution (17), it can deduce

$$c=2V_TC_5/I_B \tag{18}$$

The eqution (15) and (18) are substituted into eqution (9), it can obtain

$$\omega_0=I_B/(2V_T\sqrt{C_4C_5}) \tag{19}$$

quality factor $Q=\sqrt{C_5/C_4}$ and dc gain K=1.

so the cut-off frequency of log-domain filter is:

$$f_0=\omega_0/2\pi=I_B/(4\pi V_T\sqrt{C_4C_5}) \tag{20}$$

The eqution (6) is substituted into eqution (20), it can deduce

$$f_0=[(C_{OS}\times6.8\times10^3+3.0\times10^{-7})\times R_4]/(4\pi V_TR_9\sqrt{C_4C_5})\times f_i \tag{21}$$

It can be seen from eqution (21) that the cut-off frequency of the filter designed will change linearly with input frequency as long as adjusting the value of capacitors and resistors reasonably.

4 Experimental result

Design frequency range of the filter from 1MHz to 30MHz. When taking C_{OS} = 53pf, $C_4 = C_5$ = 1010pf, R_4 = 100Ω, R_9 = 200KΩ, R_1 = 2.2KΩ, R_2 = 20KΩ, R_3 = 250KΩ, C_1 = 1000pf, $C_2 = C_3$ = 0.1uf, C_{INT} = 3.3pf, R_{10} = 500Ω, then according to eqution（21）, it can deduce

$$f_0=f_i \tag{22}$$

The above parameters are substituted into the eqution (20), it can deduce $f_0 = 3.03\times10^9 I_B$. The input current signal is taken 500uA, the control bias current I_B are taken 330uA, 990uA, 3300uA, 6600uA, 9900uA, the simulation results with ORCAD are shown in figure 7.

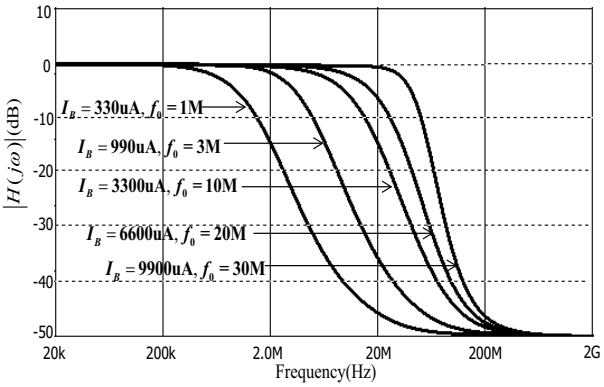

Figure 7. The amplitude-frequency responses of the log-domain second-order low-pass filter.

According to figure 7, the analysis of second-order low-pass log-domain filter performance is shown in table 1, including the bias current corresponding to the input frequency, cut-off frequency and stop-band attenuation rate.

Table 1. The performance of the filter.

Input frequency (f_i / MHz)	Bias current (I_B / uA)	Cut-off frequency (f_0 / MHz)	Stop-band attenuation rate(dB/decade)
1	330	1	40
3	990	3	40
10	3300	10	45
20	6600	20	45
30	9900	30	45

Analysis the experimental results, it can obtain: the cut-off frequency f_0 of the designed second-order low-pass log-domain filter changes along with the change of the input bias current I_B, and has a linear relationship with I_B. When the frequency of the input signal is small, the attenuation of amplitude frequency characteristics of the filter in stop-band is not very good. When the input frequency increasing, the cut-off frequency of low-pass filter also increases accordingly, the amplitude frequency characteristics within the pass-band is relatively flat, in the stop-band attenuation rate is also increasing, the attenuation is very good. Transformation precision of the transistor is the main affecting factor. Can be seen from the overall result, the cut-off frequency of second-order low-pass log-domain filter can vary with the change of the input signal frequency, namely realizing automatic adjustment of the cut-off frequency to the input signal frequency.

5 Conclusion

The design method of this paper is to convert the signal frequency into current value through the broadband F/I

circuit. The current signal, which is input into the bias current control end of the log-domain filter, controls the cut-off frequency of filter, so as to achieve automatic adaptation of the filter's frequency. The actual circuit structure is designed. When the input signal changes in frequency range from 1MHz to 30MHz, the cut-off frequency of the adaptive second-order low-pass filter can automatically adapt to the change of the input signal frequency. From software simulation test of the circuit, it can see the waveform is good, and the filter amplitude-frequency characteristics within the pass-band is relatively flat, the attenuation in stop-band is good, proved the correctness of the circuit and the validity of the design. In this paper, the designed adaptive second-order log-domain low-pass filter is mainly composed of the broadband F/I circuit, V/I circuit, transistors and a small amount of resistors and capacitors. The structure of circuit is simple and easy to adjust. And the filter system has broad filtering bandwidth, good real-time dynamic characteristics, and can be widely used in all aspects of the sensor data processing. It resolves the problem of the measured signal frequency changing in a wide range.

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