MATEC Web of Conferences **42**, 02003 (2016)
DOI: 10.1051/matecconf/20164202003

Robust Sequential Circuits Design Technique for Low Voltage and High Noise Scenarios

Lancelot Garcia-Leyva[1,3,a], Juan Rivera-Dueñas[2], Antonio Calomarde[3], Francesc Moll[3] and Antonio Rubio[3]

[1]*Universidad Autónoma de Tlaxcala, Apizaco; Tlaxcala, Mexico*
[2]*Universidad Nacional Autónoma de México, Ciudad de Mexico, Mexico*
[3]*Universitat Politecnica de Catalunya, Barcelona, Spain*

Abstract. All electronic processing components in future deep nanotechnologies will exhibit high noise level and/or low S/N ratios because of the extreme voltage reduction and the nearly erratic nature of such devices. Systems implemented with these devices would exhibit a high probability to fail, causing an unacceptably reduced reliability. In this paper we introduce an innovative input and output data redundancy principle for sequential block circuits, the responsible to keep the state of the system, showing its efficiency in front of other robust technique approaches. The methodology is totally different from the Von Neumann approaches, because element are not replicated N times, but instead, they check the coherence of redundant input data no allowing data propagation in case of discrepancy. This mechanism does not require voting devices.

1 Introduction

Fault-tolerance on semiconductor devices has been a key issue since upsets were first experienced in space applications several years ago. Since then, the interest in studying fault-tolerance techniques in order to keep the data integrity of integrated circuits operating in hostile environment has increased, driven by all possible applications of radiation tolerant circuits and the requirement of high reliability behaviour [1].

In addition, because of the continuous shrinking evolution of the technology of semiconductor components as well as the reduction of voltage levels for energy saving purposes, the increase of speed and logic density [2], the need of fault-tolerant mechanisms is becoming a key remerging topic. As stated in [3], drastic device shrinking, power supply reduction and increasing operating speeds significantly reduce the noise margins and thus the reliability that very deep submicron (VDSM) ICs face from the various internal and external sources of noise. The basis of the robust design methodology presented in this paper is based on the use of redundant data expression *L*, over the whole set of logic elements in the system. This redundant input/output data mechanism is called port redundancy and in [4] it was demonstrated that an acceptable ratio between reliability improvement and hardware overhead can be accomplished just by duplicating the input and output data ports *L*=2.

The design principle lies on the coherence enforcement of each pair of redundant inputs. All variables of input ports are expressed through their true and complement values (*L*=2), as well as their output variables, with a clear similarity with differential logic, but with behaviour of the processing blocks significantly different. In case any input port presents a discrepancy of logic values, the sequential elements holds the previous output values, hence refraining the propagation of incorrect inputs. Consequently in case of aggressions the memory elements present a shielding effect of the logic, and because of this behaviour we call the logic implemented with this principle turtle logic (TL).

2 Sequential Logic Elements

The principles of design of D-type flip-flops based on our TL implementation technique are shown in this section. We consider the D flip-flop organized from a structure of two cascaded D-Latches with complemented clock signals.

2.1 TL D-Latch design

The TL D-Latch equations for transparent (clock equal to 0) and latch (clock equal to 1) phases are given by:

- If (CLKt = 0 & CLKc = 1 & (Dt = Dc)), then
  Qlt <= Dt; Qlc <= Dc.
- Otherwise:
  Qlt <= Qltprevious; Qlc <= Qlcprevious.

Where, Dt and Dc are the two redundant input data variables, CLKt and CLKc are the true and

[a] Corresponding author: lancelotssxja@gmail.com

Article available at http://www.matec-conferences.org or http://dx.doi.org/10.1051/matecconf/20164202003

complemented signals of the clock, and Qltprevious and Qlcprevious are the output data of the previous state, Qlt and Qlc correspond to the current state. It is worth noting that the sub index *t* and *c* correspond to true and complementary signals, respectively. Figure 1 shows optimized implementation of TL D-Latch at transistor and gate level.

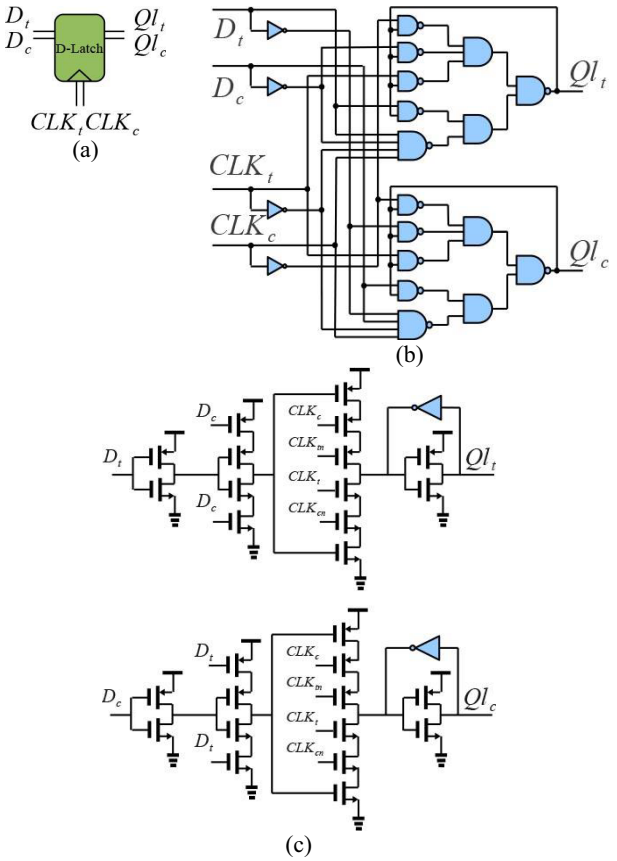

Figure 1. Implementation of a TL D-Latch at transistor and gate levels, (a) symbol, (b) logic implementation and (c) transistor level implementation.

2.2. TL D-Flip Flop design

The TL D-Flip Flop is implemented using two Turtle logic D-Latch cascaded as shown in Figure 2(b), which follows the specs of Turtle logic. The flags fdft and fdfc Figure 2(c), indicate when the output data is valid and when it is not. With the use of this Turtle logic and flip-flops it is possible to implement Finite State Machines.

The behaviour of a Turtle D-Flip Flop active in positive edge is:

- If ((CLKt ↑ || CLKc ↓) & (Dt ≠ Dc)), then

  Qft <= Dt; Qfc <= Dc.

- Otherwise:

  Qft <= Qftprevious; Qfc <= Qfcprevious.

Where, Dt and Dc are the redundant input data, CLKt and CLKc are the redundant clocks, ↑ positive and ↓ negative are edges triggered clock, Qftprevious and Qfcprevious are the output data of the previous state, and finally Qft and Qfc correspond to next state. Never mind if CLKt↑ happens before, after or during CLKc↓, the input data are not transferred to the outputs until the occurrence of both complementary clocks.

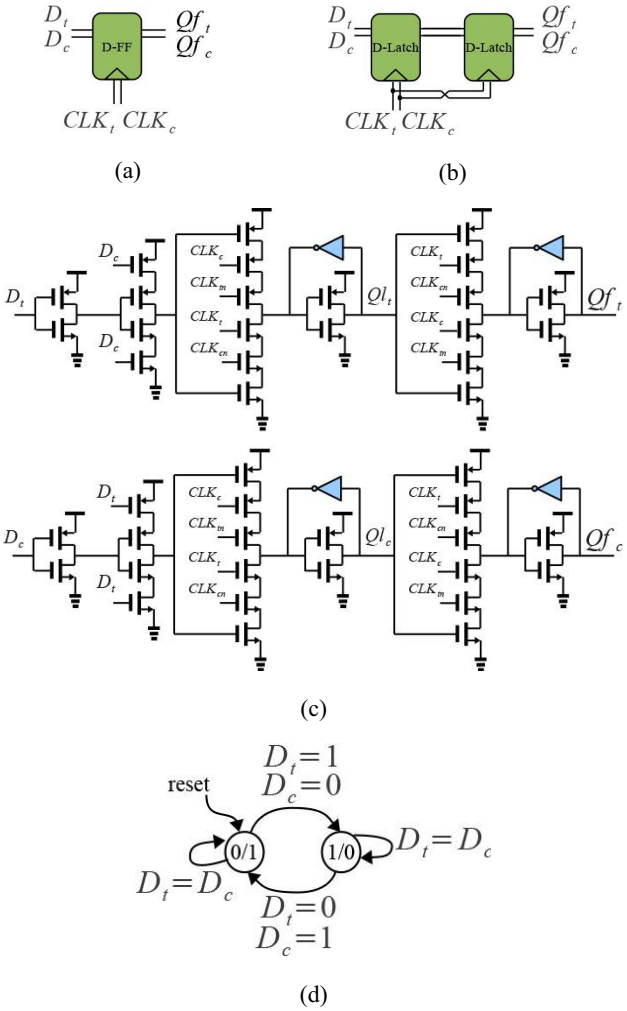

Figure 2. TL D-Flip Flop. (a) Symbol and (b) Schematic view using two D-Latch connected in cascade. (c) Transistor level design for a D-Latch, and (d) An state's machine.

2.3. Evaluation and comparison of the robustness of the TL Flip Flops

In order to evaluate and compare experimentally the robustness of the TL sequential proposal respect other techniques previously published we have implemented physically (transistor level) a D-Flip Flop circuit following five different alternatives: a conventional CMOS style, a Triple Modular Redundancy (TMR) [6], third a 1st-order Cascaded Triple Modular Redundancy (CTMR) [6], fourth a Markov Random Field (MRF) [7] proposal and finally our TL design. The experimental scenario has been based on Spice-like simulation of the respective circuits a 90nm technology device with a VDD of 0.5V at temperature of 120°C, a critical sub threshold situation for such a technology in order to force the devices to exhibit transient failures. Internal noise was generated using transient-noise option of the circuit

simulator, which generates thermal and flicker noises to each transistor channel, and shot noise to each power supply at each time step. The noise generated to each transistor and power source were amplified x100 respect to the intrinsic noise of the 90nm technology, emulating the hostile environment and behaviour of future technology with high-noise components. It is worth noting that nominal V_{DD} for this technology is 1V, but in this work it was decreased to 0.5V to emulate a weak equivalent environment in future technologies, where extremely low SNR will have a greater relevance and observe the behaviour of the different alternatives.

In the Figure 3 the noise added to the input signals were generated with independent AWGN modules implemented using Verilog-A, with 0V mean and standard deviation of 0.5 Vrms for both ``1" and ``0" logic levels as well as for CLKt and CLKc, using different seed for each input and therefore uncorrelated noisy sources. The correct outputs of the device under test are observed in spite of the extreme high noise.

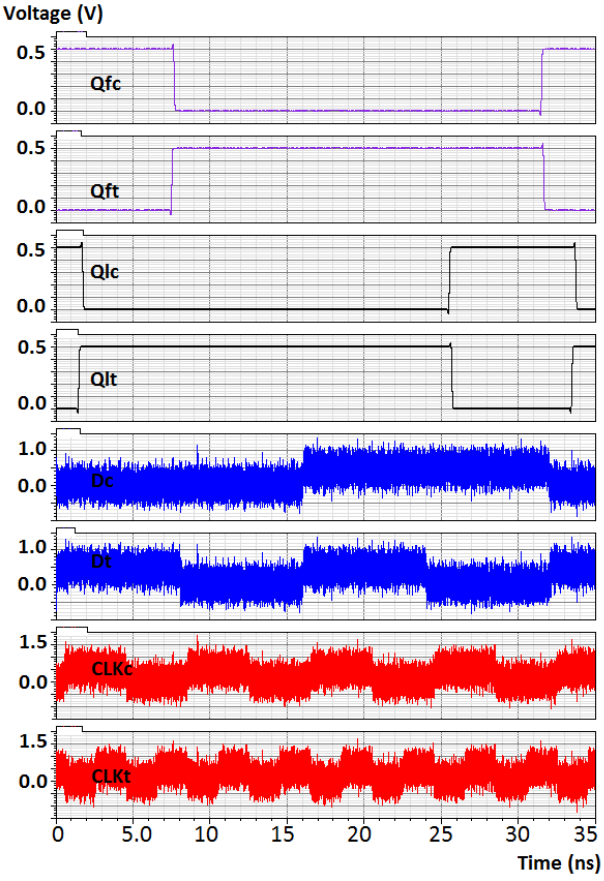

Figure 3. Simulation results (first four waveforms) of the response of a TL D- Flip Flop and D-Latch when a high level noise (0V mean and standard deviation of 0.5 V rms for both 1 and 0 logic levels with VDD=0.5 V) is added to the D and CLK inputs.

To show a numerical robustness comparison we use as robustness merit factor the Kullback Leibler distance (KLD) [5] a recognized measure of the discrepancy between two probability distributions over the same event space. The KLD of the probability distributions Pideal (ideal logic), Preal (each one of the five real experiments) on a finite input set X is defined as shown in Equation 1.

$$KLD(P_{ideal}, P_{real}) = \sum P_{ideal} * log_2(P_{ideal}/P_{real}) \quad (1)$$

It is established that the smaller the KLD measure, the better the noise immunity of the circuit being measured. Hence it can be said that a value of KLD=0 corresponds to an ideal and perfect operation of the devices. Performing a measurement of the output voltages of each 0.1ns, for the mentioned experimental cases are measured and quantitatively comparing the noise immunity of sequential logic elements.

Table 1. Comparison of error tolerance by Kullback Leibler Distance.

	CMOS	TMR	1st CTMR	MRF	TL
D-Latch	1.401	0.5913	0.4745	0.2481	0.1070
D-FF	1.2204	0.5699	0.4309	0.2190	0.0930

Table 1 shows the KLD factors for D-latch and Flip-Flop in the five cases. The TL sequential element proposal has much better error tolerance according to Kullback Leibler Distance versus Triple Modular Redundancy (TMR) [6], 1st-order Cascaded Triple Modular Redundancy (1st CTMR) [6] and Markov Random Field (MRF) [7] techniques. In terms of hardware overhead TL exhibits much better characteristics in comparison with the redundant strategies (TMR, CTMR, MRF).

Table 2 shows the hardware cost corresponding to each alternative for transistor-level circuit designs (transistors/area). Comparing with conventional CMOS, TMR, 1st CTMR and MRF, TL latch area is an order of 5.8X, 0.84X, 0.27X y 0.56X times respectively for a D-Latch and 7.0X, 1.05X, 0.34X y 0.56X times respectively for a D-Flip Flop. The first line in the Table shows the transistor number and the second line the area cost expressed in μm^2. The area cost of sequential elements treated in this section were obtained using standard cells for a gate implementation that is the worst scenario in terms of area's cost.

3 Conclusions

We have introduced a novel redundant design technique (TL) for sequential blocks showing higher robustness to noise and low voltage implications those previous proposals as TMR, CTMR or MRF. We have experienced with implemented basic sequential elements on a given VLSI technology obtaining significant robustness improvement techniques.

In the experimentation different sources of noise have been considered, thermal noise, flicker and shot in order to emulate the behaviours of future technologies. Such factors are critical to applications in communications, navigation and control. Making a comparison of noise tolerance for a D-Latch, by the Kullback-Leibler distance, which determines the discrepancy between the probability distribution of the noisy output regarding the probability distribution of the ideal output, TL proposed strategy is 2.3X, 4.4X, 5.5X and 13.1X better than the techniques MRF, 1st-order CTMR, TMR and standard CMOS, respectively. In the same way TL implementation of a D-Flip Flop presents 2.3X, 4.6X, 6.12X and 13.1X better noise robustness than the techniques MRF reinforcer, 1st-order CTMR, TMR and standard CMOS, respectively.

We show that the TL sequential elements exhibit better noise immunity according to the parameters of Kullback Leibler measure. These circuits have an additional overhead cost in its implementation respect standard CMOS but a much lower cost respect to rest techniques based on probabilistic strategies and Von Neumann architecture. Therefore, elements based on TL improve system reliability in noisy scenarios at a reasonable cost, becoming an attractive alternative.

Table 2. Overhead comparison respect a standard CMOS implementation.

	CMOS	TMR	1st CTMR	MRF	TL
D-Latch	8T	74T	248T	172T	32T
	168	1162	3641	1744	979
D-FF	17T	128T	410T	334T	64T
	275	1866	5752	2386	1958

Acknowledgments

This research work has been supported by the Spanish Ministry of Science and Innovation (MICINN) through projects TEC2008-01856 and PLE2009-0024, and Government of Mexico under grant 164013 CONACyT and UATLX-235 PROMEP.

References

1. R.D. Shrimpf, D. M. Fleetwood, "Radiation Effects And Soft Errors In Integrated Circuits And Electronic Devices", ISBN 9812389407.
2. S.Y. Wu, C.Y. Lin and J.J. Liaw, "Advancing foundry technology with scaling and innovations", Proceedings of the IEEE International Symposium on VLSI Technology, System and Application (VLSI-TSA). 2014, 1-3. doi: 10.1109/VLSI-TSA.2014.6839696.
3. A. Johnston, "Scaling and Technology Issues for Soft Error Rates", Proceedings of the 4th Annual Research Conference on Reliability, Stanford University, October 2000.
4. Garcia, L. [et al.]. "Turtle Logic: A new probabilistic design methodology of nanoscale digital circuits". Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS). 2010, 1101-1104. doi: 10.1109/MWSCAS.2010. 5548845.
5. S. Kullback, R. A. Leibler: "On information and sufficiency", The Annals of Mathematical Statistics, vol. 22, No. 1, pp. 79-86, 1951.
6. O. Roystein, J. Aditya, and J. C. Tapan, `A tmr scheme for seu mitigation in scan flip-flops', Proceedings of the 8th International Symposium on Quality Electronic Design, IEEE Computer Society, 2007.
7. K. Nepal, R. Bahar, J. Mundy, W. Patterson, and A. Zaslavsky, `The MRF Reinforcer: A Probabilistic Element for Space Redundancy in Nanoscale Circuits', Micro, IEEE (Volume:26, Issue: 5), Sept.-Oct. 2006, pp. 19-27.