CMOS Pixel Spectroscopic Circuits for Cd(Zn)Te Gamma Ray Imagers

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Abstract. A family of 2-D pixel CMOS ASICs have been developed to be used as readout electronics of gamma ray imaging instruments based on hybrid pixel sensor arrays. One element of the sensor array consists of a pixilated single crystal of CdTe or CdZnTe semiconductor bump bonded to the CMOS electronic circuit. The first member of the family can process single photon signals which deliver up to 4fCb charge, while the two other can process signals up to 36fCb. A unique readout mode and the simultaneous extraction of energy and time tagging information of the converted photons differentiate the members of this family from other existing CMOS readout circuits.

1 Introduction

Compound semiconductor sensors, mainly CdTe/CdZnTe, find steadily increasing application in room – temperature, large volume X/Gamma-ray imaging coupled with spectrometry in the security [1], medical[2], industrial[3] and space sectors[4]. They are attractive because direct conversion of the gamma photons to electric signal exterminates all the problems of spatial localization related to light diffusion which is unavoidable in the scintillating crystal, (silicon) photomultiplier couple. In addition their energy resolution is far superior from the combination of scintillation crystals and photomultipliers and lithography can be used to pattern electrodes with very fine pitch. The art of production of single crystal binary and ternary compound semiconductors is advanced steadily. This renders possible the development of less bulky devices operating at room temperature.

The traditional gamma camera design, based on a NaI-scintillator and photomultiplier tubes, has about 50 electronic channels per 0.25m². As one tube corresponds to one electronic channel, the number and the density of channels makes the implementation of the front-end readout electronics using discrete components a natural solution. But new cameras using compound semiconductors as sensing layer have many electrodes, in the form of pixels or strips. Due to the large number of channels, front-end electronics is implemented in the vicinity of the sensor using integrated circuits with sub-micron feature size. Those imaging systems are read out by custom-made application specific integrated circuits (ASICs). These ASICs are designed and manufactured

mainly in complementary metal-oxide-semiconductor (CMOS) technology.

Also interconnection of CdTe/CdZnTe sensors having high pin count with the electronics is a challenging task and it is performed with a process, which is called “hybridization”. Bumps on either the detector pixel side or the CMOS readout ASIC pixel side or on both of them are developed and then thermo-compression of the detector to the CMOS is applied. Conventional solder flip chip assembly is not a practical option, since Cd(Zn)Te detectors are limited to processing temperatures below 100°.

Figure 1 (a) Bi/Sn bumps developed on the in-pixel pads, (b) The hybrid detector module

The process begins with vacuum deposition of an Under Bump Metallization (UBM) layer over the metal pads of one or both surfaces to be joined. Indium, Bi/Sn or other metals are deposited onto the UBM metal using either a shadow mask or photoresist lift-off technique to define the bump geometries. The bumps are typically

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only 15-20 μm in diameter and 7-10 μm thick, resulting in the surfaces being separated by only 8-15 μm after assembly. Flatness of the surfaces and uniformity of the bump heights are critical to the success of this process. The hybrid shown in Figure 1 has detecting layer made of 2mm thick CdTe with “ohmic type” electrodes.

2 Specifications

Our development is driven by the constraints imposed by the task to identify the radioactive source species and its spatial coordinates. In other words we try to discriminate from where emanate and what is the “color” of the gamma ray photons impinging our device. Two methods are in use for this purpose: the one is called coded aperture imaging [5] and the other Compton imaging [6]. The identification of the radioactive source calls for the determination of the energy of the converted photons, i.e. every channel of the readout electronics should be able to give spectroscopic information.

In coded aperture imaging a coded aperture (mask) is placed on top of a position sensitive gamma-ray detector. A nuclear source located within the field of view of the camera illuminates a sub-region of the mask and consequently produces shadow patterns on the detector. The source direction is inferred by the de-convolution of the recorded images. This imposes the necessity of having the x-y information of the photon counts.

Instruments that exploit the Compton imaging technique deduce the energy of the incident gamma ray photons as well as their origin within a cone, by measuring the energy depositions and the positions of the Compton scattering interactions recorded in the detector. Successive interactions of the emitted gamma rays create overlapping cones and the source location is the intersection of all measured cones. The determination of the correct sequence of photon interactions in the detector is crucial. The reason can be easily visualized in the case of a fully absorbed photon interacting in the active parts of the detector via a Compton scattering (dual hit event), as is illustrated in Figure 2 [7].

Consequently the spatial information of the hit, energy and time tagging capability are required. The energy resolution is connected to the FWHM of the distribution of the difference between the angle of direction of the photon emanating from a radioactive source calculated by using the Compton formula and the real one.

The detector layer affects the design of the pixel electronics through many routes:

(a) The pixel capacitance is an important parameter for the design, because (a) the total capacitance of each pixel determines the noise of the preamplifier and the inter-pixel capacitance determines the cross-talk between pixels. We calculated and measured the capacitance of the pixels of two different kinds of CdTe pixel detectors [8]. The fair agreement between measurement and calculations in these cases gave us confidence to repeat the calculations for the detector with pixels of 400 μm pitch. It should be noted that the capacitance measurements could not take into account the fact that when the ASIC is bump bonded to the detector its top

metal layers come close to the detector pixel (the distance between the detector and the ASIC is around 15 μm). This results to a charge redistribution which affects the capacitance dramatically. We simulated this effect and the capacitance was 6 times larger than without taking this into account. In conclusion the total capacitance at the input was assumed 600pF.

Figure 2 Compton sequence reconstruction of an event with two hits in the active detector's volume. Incorrect determination of the hit sequence results to wrong estimation of the Compton angle.

(b) The peaking time of the shaper amplifier within the pixel electronics should not be less than the charge collection time. The charge collection time was estimated [8] and we were led to the decision to implement programmable peaking time with range from 0.5 μs to 2 μs .

(c) The mean energy for the creation of an electron-hole pair for CdTe is 4.43 eV. In the first CMOS readout circuit the upper limit of the charge signal to be processed by the pixel low noise amplifier was set to 4fCb which corresponds to photon energy of 110 KeV. The other two circuits have a limit of 36fCb corresponding to 800KeV photon energy.

(d) The fraction of the leakage current of the detector is a function of the detector type (Schottky or Ohmic), material resistivity, bias voltage, pixel area and it can reach a value of several nA. Also the direction of leakage current flow does matter in the design of the first stages of the pixel electronics. In the first CMOS readout circuit both the leakage current and the signal which can be applied are positive, where positive means current direction towards the input of the charge amplifier. This implies that we restrict to detectors with positive bias voltage. Also in that circuit we did not implement any mechanism for the compensation of the effect of the leakage current. In the other two readout circuits a leakage current compensation mechanism was implemented and the direction of the input current flow can be either towards or outwards the input of the first stage. A polarity selection mechanism is configured at the initial stage of the operation of the electronics according to the polarity of the bias voltage of the crystal connected to it.

The same hybrid as the one shown in Figure 1(b) has been constructed by using 0.75mm thick CdTe crystal but with electrodes which create Schottky type diodes on the surface between the pixel electrode and the CdTe bulk.

As the CdTe material is p-type doped, the pixel electronics receive signal from gamma ray sensitive diodes. The diodes should be reverse biased and the high

resistivity of CdTe calls for high voltage bias (a nominal value is -500V) in order to assure both the full depletion of the bulk and the full charge collection.

The CMOS readout circuits are called P4DI, the acronym of Photon 4-dimensional Digital Information and they are shown in Fig. 3. The first version (P4DI_v1, Figure 3(a)) and the second version (P4DI_v2, Figure 3(b)) have 64 pixels organized in 8 rows by 8 columns, while the third member (P4DI_v2F, Figure 3(c)) has 50 rows x 25 columns, which means 1250 pixels. The pixel pitch in all the ASICs is 400 μ m. At the bottom of the pixel array there are circuits common to a column. A controller embedded in the ASIC coordinates the different phases of operation: Initialization, hit recording period, A/D conversion, data readout. The ASICs have been implemented in the UMC 0.18 μ m mixed signal process technology.

3 Pixel Functionality and Results

The information provided by each pixel is a voltage level proportional to the charge delivered by the current pulse of the detector pixel and a voltage level proportional to the time interval between the assertion of the hit flag and the arrival of an external reference signal. These two voltage levels can be digitized in the pixel with 10 bits resolution and sent outside the chip together with the digital pixel address. Alternatively the two voltage levels can be sent in analog form to the outside of the chip and digitized externally. Only pixels with hit information are readout. Initialization and data readout are performed in a serial manner.

The pixel layout is shown in Figure 4. It has an analog and a digital part. The analog part contains a charge amplifier whose output is connected to the input of a polarity select circuit. This circuit can invert the output of the charge amplifier if an initial configuration bit is set. A leakage current compensation op-amp samples the output of the charge amplifier and compares it to the output of an in-pixel low power replica of the charge amplifier circuit with identical bias. Its output signal is driven to a low pass filter which controls the value of a current source – sink connected to the input of the charge amplifier. This current source-sink cancels the detector's leakage current. The output of the charge amplifier either inverted or not is connected to a CR-RC shaper with variable gain and peaking time, both set with 3 configuration bits.

A comparator compares the output of the shaper to the baseline voltage produced by an in-pixel low power replica of the shaper and augmented by 25 more or less mV. A current pulse from the detector forces the comparator to fire and initiate a sequence of actions to be taken by the digital part of the pixel. One of these actions is to set the in-pixel peak detection and hold circuit in its hold mode. The peak detection circuit input is provided by the shaper. The held voltage is the one of the two outputs produced by the pixel.

The triggered digital part of the circuit starts the operation of a circuit residing in the analog part of the pixel and producing a voltage ramp. The voltage ramp

stops when the externally provided signal which starts the analog to digital conversion is asserted. Consequently this circuit plays the role of a time to voltage converter producing a time stamp in the form of a dc voltage level, which is the second output produced by the pixel.

(a)

(b)

(c)

Figure 3 The P4DI family (a)P4DI_v1, (b)P4DI_v2, (c) P4DI_v2F.

Spectra (distributions of the pulse heights) recorded by two neighbor pixels are presented in Figure 5. The spectra are collected when photons emitted from Am241 and Co57 radioactive sources hit the pixilated CdTe crystal connected to the P4DI_v2F. Also spectra resulting from test pulses injected to the same pixels are superimposed. The test pulse voltages were adjusted to deliver the same charge to a 52fF capacitance, which is the nominal value of the in pixel test capacitor, as that delivered by 59.54KeV and 122KeV photons. It is clear from the coincidence of the centroids of the test pulses with those from the recorded photon hits that almost full

charge collection is achieved. One can see that photon hits appear above different voltage thresholds in the two pixels. In the one of the pixels counts appear beyond 950mV, while in the other counts appear beyond 925mV. This is due to the fact that the hit flag comparator threshold is not set globally, but it is set by design in each pixel separately to be 20mV above the baseline of the in-pixel shaper.

Figure 4 The pixel layout

4 Conclusions

The functionality of a 2 dimensional array of spectroscopic channels with 1250 elements with 400um pitch has been proven. Taking into account the fact that time tagging information is provided simultaneously with the energy information and low power consumption has been achieved (200uW/channel), the result of the presented work is a family of CMOS circuits capable to cope with the requirements of truly portable, low form factor gamma ray imagers for Compton and coded aperture imaging.

Figure 3 Pulse height distributions (spectra) either of gamma photons or of test pulses recorded from neighbor pixels .

Acknowledgment

We thank A. Nikologiannis for his work in the embedded controller of P4DI v1 and I. Papadakis and I. Kazas for the development of the test setup for these circuits.

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