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The Implementation of E1 Clock Recovery

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Abstract. Clock transform and recovery is of significant importance in microwave TDM service, and it is always extracted from the E1 line data stream in most cases. However, intrinsically uncertain delay and jitter caused by packet transmission of E1 data information, may lead to the indexes of the data recovery clock exceed the clock performance template. Through analysis of the E1 clock indexes and measuring methods, this paper proposes a new clock recovery method. The method employs two buffers, the first RAM is used as a buffer to deduct excess information, and the second FIFO is used as a buffer to recovery the clock and data. The first buffer has a feedback from the second one, and is able to actively respond to changes in the data link and requests from the second one. The test results validate the effectiveness of the method, and the corresponding scheme is also valuable for the other communication systems.

1 INTRODUCTION

E1 data transmission standard [1,2,3] defines the criterion of jitter and wander, and provides the related index template about E1 digital timing sequence. The equipment indexes exceeding these templates would induce equipment code slip bit errors and so on. Specifically, when the timing signal deviates from its optimal location, an error is possible to be emerging during the signal recovery and reconstruction process[4]; when the equipment could not tolerate an error between the output and input clock signals (frequency and phase), a skip code will happen.

The stability index of the E1 service clock is called Wander, which is a slow phase modulation of the time information (the frequency spectral component is lower than 10Hz) and is generated by the dynamic buffers in the whole transmission network [5].

In order to acquire the information related to wander, three parameters are required to analyze: TIE, MTIE and TDEV.

TIE (Time Interval Error), is an indicator of the amplitude about the phase change.

MTIE (Time Interval Error Maximum) is the maximum peak-to-peak value of TIE during a certain observation time. MTIE's value can be used to determine the capacity of buffer in synchronous systems. The buffer associated with the PLL can absorb a part of the frequency fluctuation. Whereas, increasing capacity of buffer will increase system delay correspondingly. From practical perspective, the number of buffer is determined according to the actual effect.

TDEV (Deviation Time) is the measurement of the TIE signal, characterized by its spectral components.

Based on definition of these three physical quantities (TIE, MTIE, TDEV), the limit imposed by MTIE reveals that TIE should not have dramatic changes in the duration of observation time. As a result, the period of TIE should be kept within certain limits, and the MTIE template can pass; As to TDEV index, restrictions (upper limit) require that the fluctuation frequency energy is suppressed. If the TIE keeps constant, there is only initial phase between the recovery and the reference clocks, TDEV index will become ideal without fluctuation [6]. If TIE changes monotonously (increase or decrease linearly), it shows that there is a fixed frequency difference between the recovery and the reference clocks. In this condition, MTIE will increase without limit and clock recovery needs to be corrected. TDEV template defines the additional wander of the clock signal and provides the tracking degree between the recovery and the reference clocks; when the index exceeds the requirements, it shows that the recovery clock has deviated far away from the reference clock.

2 The Raise of the Problem

In the process of testing microwave equipment, the output of the device's E1 clock is tested in the PDH mode according to the relevant standards, and the test block diagram is shown in Figure 1. The results of three indicators in PDH mode are shown in Figure

2, Figure 3 and Figure 4, respectively, displaying the changes of clock indexes.

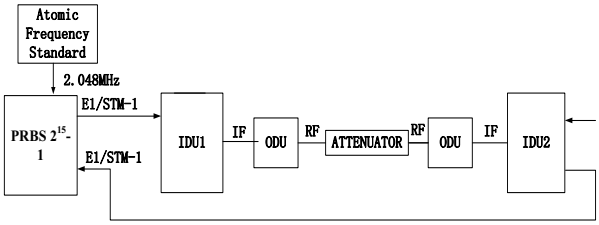

Figure 1. Test system of the E1 output wander

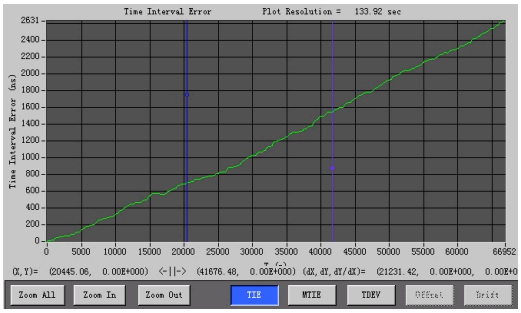

Figure 2. TIE of the original scenario

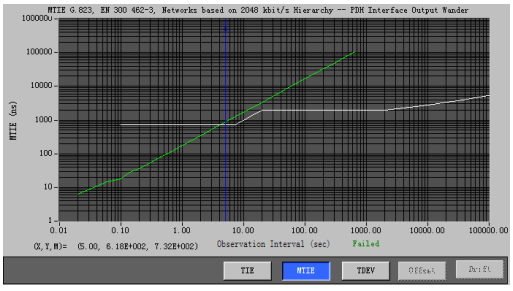

Figure 3. MTIE of the original scenario

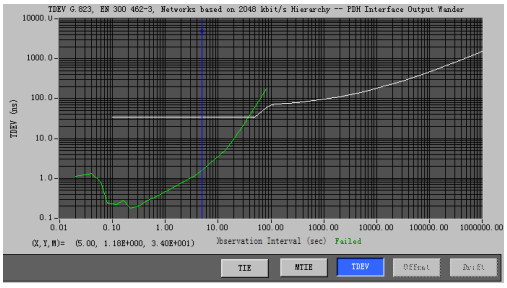

Figure 4 .TDEV of the original scenario

Obviously, TIE increases monotonously, but not evenly, showing that there is not only frequency offset between the recovery clock and the reference clock but also phase modulation caused by noise. Meanwhile, MTIE diagram reveals a similar one-way linear. Besides, from TDEV diagram, noise components increasing with observation time becomes obviously and exceeds the template [7]. The recovery clock is from the E1 of the microwave service, and the reference clock is from rubidium atomic clock. Therefore, it is necessary to carry on the analysis to the strategy of the clock in the original scenario.

3 Proposed solution and implementation

3.1 Original Clock Strategy

The factors influencing clock index include: the code rate adjustment in initial data transmission, the buffers of the intermediate levels, and the data buffers of clock recovery.

In the transmission direction, the adjustment of code rate introduces a modulation effect, and temporary storage in the downlink RAM may cause timing error. After the adjustment of the code rate, the time error would bring in external delay. Standard 2.048Mbit/s E1 data streams with time information are recovered from numerous errors by final clock recovery module, according to the input and local reference clock. The recovered clock is required to track the changes of the input clock and satisfy the corresponding TDEV and MTIE targets.

According to the amount of data in the uplink RAM, the original clock recovery uses a sigma delta algorithm to determine whether to increase the pulse of the reference clock, and then sends the upstream RAM data with the recovered clock, as shown in Figure 5. When the RAM data exceeds the established upper limit, the standard pulse deduction operation is accelerated, and the recovery clock speeds up. When the RAM data is under the lower limit, the standard pulse deduction operation is slow; meanwhile, the recovered clock frequency is reduced and the data readout rate slows down. When the data lies between the lower and upper limits, the standard readout pulse is not treated in order to achieve the purpose of tracking the input clock.

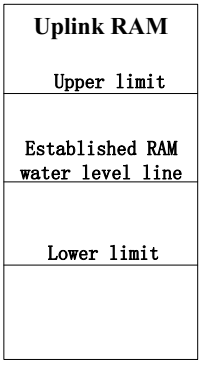

Figure 5. The direct recovery data from the uplink RAM

The writing rate of RAM is 2.072MHz, and there is no operation for the bit of adjusted data. In the process of clock recovery, the deduction process of a bit stream is performed (the inverse process of initial rate adjustment). The results show that the TDEV index is over gauge, which indicates that the upper and lower limits of the reservation are too large to be reduced. The smaller the range is, the more sensitive the change of the input rate is, and the more quickly the input clock is tracked [8]. And then, the long wander is suppressed, and there would be a good

TDEV index. Based on this view, the following scheme is designed:

1) The original design has an adjustable upper and lower rang, and then the changed design should reduce and fix the adjustment range (upper and lower limits).

2) On the basis of the uplink RAM, a small FIFO is added to the second clock recovery. The RAM data is read out in accordance with the rate of 2.072MHz, and then the bit stream deducted is filled into the FIFO, the FIFO data bit is imported with pure E1 data, the FIFO is used to restore a clock that matches to the rate of the input clock.

3.2 The Adjustment of the Clock Strategy

Although reducing the dynamic range seems to improve the TDEV index, the recovery process is mixed with rate adjustment and becomes not pure. Considering the frequency difference up to 24 kHz between 2.048MHz and 2.072MHz, the effect of the adjusting rate process in clock recovery is catastrophic. The recovery process of the two-level clocks is shown in Figure6. Only a small FIFO is added to the first RAM. The rate adjustment process and the clock recovery are independent, and only a simple E1 data exists in the FIFO with no inserting bits. The first RAM sets a limit in the middle and a deduction pulse step, and the second FIFO is also at the same way. So the input rate reacts to fill up the second FIFO, and speed tracking is obtained. The second FIFO's adjusting step size and the adjusting frequency should be greater than uplink RAM's 2.072MHz clock, otherwise uplink RAM would be read empty.

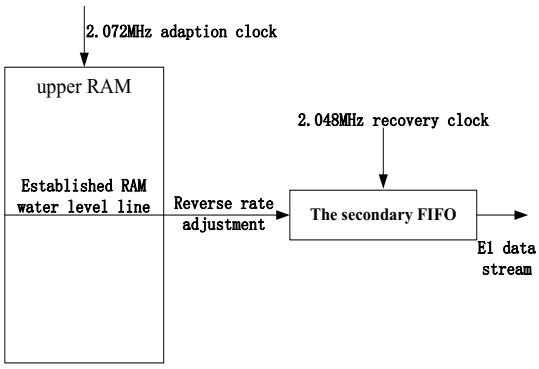

Figure 6. Schematic diagram of the two-level clock recovery

However, the adjustment steps of the buffer clocks are designed to be reconfigurable, so it is difficult to find an ideal value.

Then, the original restoration scenarios is analyzed: the first RAM with large storage space, serves as a data storage pool, and resists the flow changes on the link. The second FIFO is used only for data recovery, and the clock adjustment range is very large under normal circumstance. When the first RAM is large enough, the FIFO data filled in the second buffer would be very smoothly, and the recovery clock will not exceed the standard limits according to the internal water level, because the recovery would also be standard when the filling is with the standard rate. If the recovery doesn't meet the requirements, it indicates the problems of deduction process. Most possibly, the second FIFO is empty.

By adding the monitoring information to all levels of the data buffer, it can be found that a phenomenon of reading empty occurs in the second FIFO. Further detection verifies that TDEV index is deteriorated sharply when the second small FIFO data is read empty.

According to the analysis, if the second FIFO data recovery is continuous without interruption, the recovery process is just a pure E1 data recovery. Equivalently, the small FIFO is filled from the sender, while the receiver recovers the clock and data directly. Therefore, a new improved solution for the problem can be found: the two-level buffers are combined together by using a feedback signal. In this solution, the data is buffered and deducted in the firstly RAM, and the clock and data are recovered in the second small FIFO.

3.3 Improved results

The improved solution will be explained as follows: a monitor of the second FIFO is added to the first RAM, and the second FIFO is filled faster when the data level exceeds its limit, which ensures clock recovery is uninterrupted during the whole process. On the other hand, this solution can be seen as the feedback from the second buffer to the first one. In this term, the first buffer can respond to changes in the link actively, and reflects the changes through the second buffer, and in addition has an active response to request of data from the second buffer. The clock recovery schematic diagram improved is depicted in Figure 7. The test results show that the problem is solved effectively.

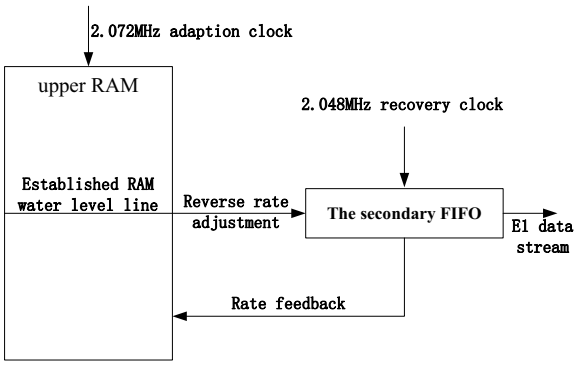

Figure 7. Schematic diagram of the improved two-level clock recovery

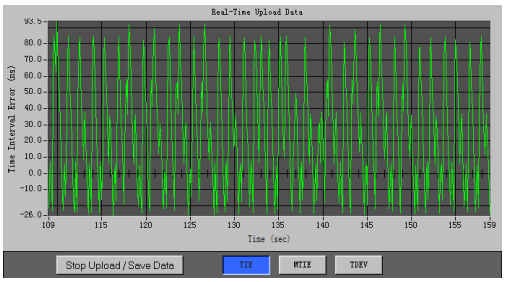

Figure 8. TIE of final scenario

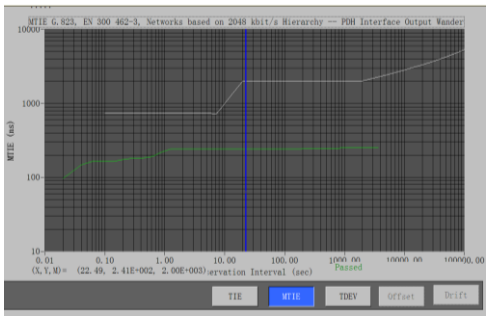

Figure 9. MTIE of final scenario

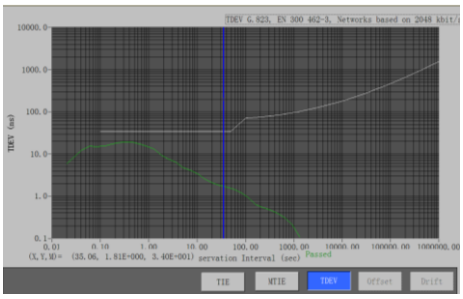

Figure 10. TDEV of final scenario

As shown above, after the fusion of the two-level recovery buffers, both the transmission rate changes and clock tracking requirements can be taken into account at the same time, and then the clock wander of the system transfer on the data can be eliminated effectively. From the measured result of the TIE, the clock recovery module keeps tuning slightly according to the amount of second buffer, and brings positive and negative fluctuations of the TIE value. From the index of MTIE in a very long time, TIE fluctuation range is within the scope of the template; the final recovery clock in frequency and time tends to the standard reference clock eventually, the TDEV index decreases with increasing time. From Figure 8, Figure9, and Figure10, it is clear that the improved scenario achieves the desired effect.

4 Conclusion

Through the analysis and resolution of the E1's clock indexes such as TIE, MTIE, and TDEV in microwave system, the physical implication is explicit, and these analysis methods are also applicable for other telecommunication systems. The two-level clock recovery modes can solve conflict between the suddenly large capacity and the rapid reaction effectively. Besides, these methods are beneficial to the other transmission systems.

Furthermore, better wander indexes can be obtained by applying multilevel buffers of the clock recovery, but the delay will be increased. So it needs to be carefully considered about the indexes and the delay on different systems.

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