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DC Bus Control of Back-to-Back Connected Two-Level PWM Rectifier-Five-Level NPC Voltage Source Inverter to Torque Ripple Reduction in Induction Motor

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Abstract. This paper proposes a regulation method of back-to-back connected two-level PWM rectifier-five-level Voltage Source Inverter (VSI) in order to reduce the torque ripple in induction motor. First part is dedicated to the presentation of the feedback control of two-level PWM rectifier. In the second part, five-level Neutral Point Clamped (NPC) voltage source inverter balancing DC bus algorithm is presented. A theoretical analysis with a complete simulation of the system is presented to prove the excellent performance of the proposed technique.

1 Introduction

The effects of torque ripple are particularly undesirable in some demanding motion control and machine tool applications. They lead to speed oscillations which cause deterioration in the performance. In addition, the torque ripple may excite resonances in the mechanical portion of the drive system, produce acoustic noise, and, in machine tool applications, leave visible patterns in high-precision machined surfaces [1].

This paper investigates the use of a back-to-back connection of two-level PWM rectifier-five-level Voltage Source Inverter (Fig. 1). This connection allow balancing of the DC link capacitor voltages under a full range of operating conditions [2] whereas, only a limited operating range is possible if a passive rectifier (diode bridge) is employed [3]. Additional advantages brought by the back-to-back connection have been shown to include: the ability to draw almost sinusoidal currents from the supply, the input power factor can be controlled and the back-to-back topology automatically regenerates power back to the supply when the operating conditions dictate [4]. Alternatively, a passive rectifier draws a pulsed current from the supply and does not allow a regenerative current to return to the supply.

In this paper, first part is dedicated to the presentation of three phases two-level PWM current rectifier regulation loop. After that the DC bus voltages balancing using the redundant vectors of five-level NPC inverter is explained. At the end the simulation results demonstrate efficacy of this of back-to-back converters DC bus control.

2 Feedback control of two-level rectifier

In this part, one proposes to enslave the output DC voltage of two-level PWM current rectifier using a PI-based feedback control. The synoptic diagram of two-level PWM current rectifier control is shown in Fig. 2. The transfer functions $G_I(S)$ and $G_V(S)$ are expressed as follows:

$$G_I(S) = \frac{(1/R_r)}{1+(L_r/R_r)S} \tag{1}$$

$$G_V(S) = \frac{1}{CS} \tag{2}$$

The modeling of this loop is based on the instantaneous power conservation principle with no loss hypothesis. This loop imposes the root mean square (rms) value of network current.

Input and output powers are:

$$\begin{cases} P_{in} = \sum_{i=1}^{3} (V_{si}\, i_{reci0} - R_r i_{reci0}^2 - \frac{L_r}{2}\frac{di_{reci0}^2}{dt}) \\ P_{out} = U_{cm}(i_c + i_{load}) \end{cases} \tag{3}$$

Different quantities i_{load}, i_c (Fig. 2) are defined as follows:

$$\begin{cases} i_{load} = \frac{2i_{d2} + i_{d1} - 2i_{d4} - i_{d3}}{4} \\ i_c = I_{recm} - i_{load} \\ U_{cm} = U_{c1} + U_{c2} + U_{c3} + U_{c4} \end{cases} \tag{4}$$

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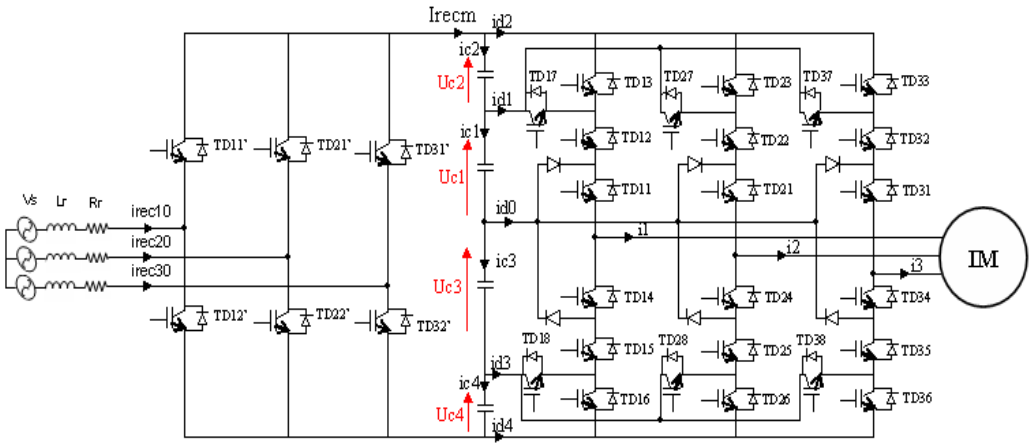

Figure 1. Two-Level PWM Rectifier-Five-Level NPC VSI Back-to-Back - Induction Motor

Using of the power conservation principle and neglecting of joules loss in the resistor R_r, and considering a sinusoidal supply network current in phase with corresponding voltage V_{si}, it can be written:

$$3V_{si}i_{reci0} = U_{cm}(i_c + i_{load}) \quad (5)$$

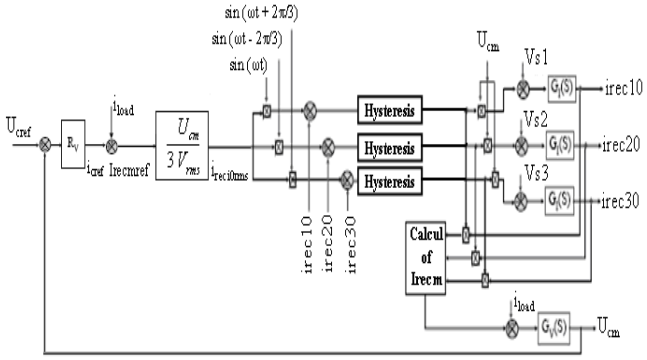

Figure 2. Synoptic diagram of two-level PWM current rectifier control

3 Simplified SVPWM of five-level NPC VSI

The space vector diagram of a five-level inverter can be considered to be composed of six hexagons that are the space vector diagrams of the three-level inverters. Each of these six hexagons, constituting the space vector diagram of a three level inverter, centers on the six apexes of the medium hexagon as shown in Fig. 3.

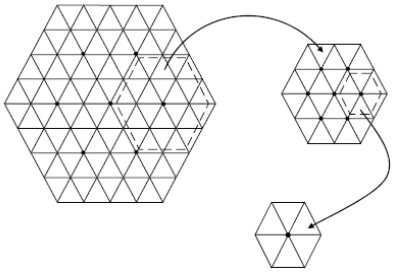

Figure 3. Simplification of a five-level space vector diagram into two-level space vector diagram

To simplify into the space vector diagram of a three-level inverter, two steps have to be taken.

Firstly, from the location of a given reference voltage, one hexagon has to be selected among the six hexagons. There exist some regions that are overlapped by two adjacent hexagons. These regions will be equally divided between the two hexagons as shown in Fig. 4. Each hexagon is identified by a number S defined in equation (6).

$$s = \begin{cases} 1 & if \quad -\pi/6 < \theta < \pi/6 \\ 2 & if \quad \pi/6 < \theta < \pi/2 \\ 3 & if \quad \pi/2 < \theta < 5\pi/6 \\ 4 & if \quad 5\pi/6 < \theta < 7\pi/6 \\ 5 & if \quad 7\pi/6 < \theta < 3\pi/2 \\ 6 & if \quad 3\pi/2 < \theta < 11\pi/6 \end{cases} \quad (6)$$

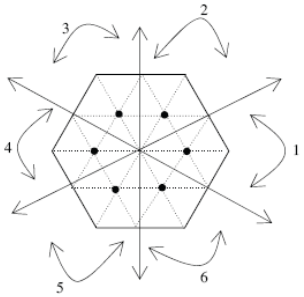

Figure 4. Division of overlapped regions

Secondly, we translate the origin of the reference voltage vector towards the center of the selected hexagon as indicated in Fig. 5. This translation is done by subtracting the center vector of selected hexagon from the original reference vector. Tab. 1 gives the components d and q of the reference voltage V^{3*} after translation, for all the six hexagons. The index (^{5}) or (^{3}) above the components indicate five or three-level cases respectively.

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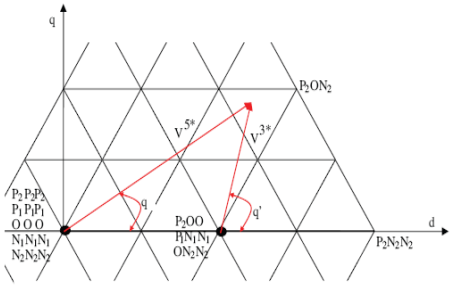

Figure 5. Translation of five-level reference voltage vector

Table 1. Correction of five-level reference voltage vector

s	v_d^{3*}	v_q^{3*}
1	$v_d^{5*}-1/2$	v_q^{5*}
2	$v_d^{5*}-1/4$	$v_q^{5*}-\sqrt{3}/4$
3	$v_d^{5*}+1/4$	$v_q^{5*}-\sqrt{3}/4$
4	$v_d^{5*}+1/2$	v_q^{5*}
5	$v_d^{5*}+1/4$	$v_q^{5*}+\sqrt{3}/4$
6	$v_d^{5*}-1/4$	$v_q^{5*}+\sqrt{3}/4$

To simplify into the space vector diagram of a two level inverter, we have to take the two steps mentioned above. Fig. 6 shows the translation of three-level reference voltage vector. The correction of its reference voltage vector is presented in Tab. 2.

Table 2. Correction of three-level reference voltage vector

s	v_d^{2*}	v_q^{2*}
1	$v_d^{3*}-1/4$	v_q^{3*}
2	$v_d^{3*}-1/8$	$v_q^{3*}-\sqrt{3}/8$
3	$v_d^{3*}+1/8$	$v_q^{3*}-\sqrt{3}/8$
4	$v_d^{3*}+1/4$	v_q^{3*}
5	$v_d^{3*}+1/8$	$v_q^{3*}+\sqrt{3}/8$
6	$v_d^{3*}-1/8$	$v_q^{3*}+\sqrt{3}/8$

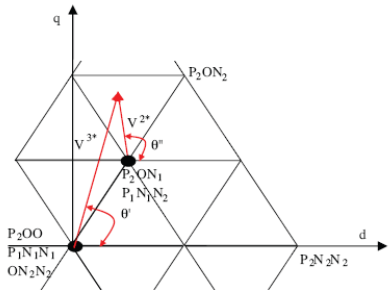

Figure 6. Translation of three-level reference voltage vector

4 Five-level NPC VSI balancing DC bus

In this part, one uses the redundant vectors of five-level NPC VSI to balance DC bus voltages [5]. Since each leg has five possible switching states, five-level inverter has 5^3 = 125 states. Some positions of output voltage vector are synthesized by more than one switching state. In Fig. 7 and Tab. 3, we can find 24 positions with no redundancy (V37 to V60), 18 positions with two redundancies (V1 to V18), 12 positions with three redundancies (V19 to V30), 6 positions with four redundancies (V30 to V36) and 1 position with five redundancies (V61).

To know the impact of each vector on capacitors voltages, four steps must be followed:

First one consists in definition of equations representing capacitors currents (i_{c1}, i_{c2}, i_{c3} and i_{c4}) as a function of load currents (i_1, i_2 and i_3) (Fig. 1) for each vector with redundant states.

Table 3. Redundant vectors of a five-level inverter

Vect		Redundancies	Vect		Redundancies	Vect		Redundancies
V1	a	P2N1N1	V19	a	P2OO	V31	a	P2P1P1
	b	P1N2N2		b	P1N1N1		b	P1OO
V2	a	P2ON1		c	ON2N2		c	ON1N1
	b	P1N1N2	V20	a	P2P1O		d	N1N2N2
V3	a	P2P1N1		b	P1ON1	V32	a	P2P2P1
	b	P1ON2		c	ON1N2		b	P1P1O
V4	a	P2P2N1	V21	a	P2P2O		c	OON1
	b	P1P1N2		b	P1P1N1		d	N1N1N2
V5	a	P1P2N1		c	OON2	V33	a	P1P2P1
	b	OP1N2	V22	a	P1P2O		b	OP1O
V6	a	OP2N1		b	OP1N1		c	N1ON1
	b	N1P1N2		c	N1ON2		d	N2N1N2
V7	a	N1P2N1	V23	a	OP2O	V34	a	P1P2P2
	b	N2P1N2		b	N1P1N1		b	OP1P1
V8	a	N1P2O		c	N2ON2		c	N1OO
	b	N2P1N1	V24	a	OP2P1		d	N2N1N1
V9	a	N1P2P1		b	N1P1O	V35	a	P1P1P2
	b	N2P1O		c	N2ON1		b	OOP1
V10	a	N1P2P2	V25	a	OP2P2		c	N1N1O
	b	N2P1P1		b	N1P1P1		d	N2N2N1
V11	a	N1P1P2		c	N2OO	V36	a	P2P1P2
	b	N2OP1	V26	a	OP1P2		b	P1OP1
V12	a	N1OP2		b	N1OP1		c	ON1O
	b	N2N1P1		c	N2N1O		d	N1N2N1
V13	a	N1N1P2	V27	a	OOP2			
	b	N2N2P1		b	N1N1P1			
V14	a	ON1P2		c	N2N2O			
	b	N1N2P1	V28	a	P1OP2			
V15	a	P1N1P2		b	ON1P1			
	b	ON2P1		c	N1N2O			
V16	a	P2N1P2	V29	a	P2OP2			
	b	P1N2P1		b	P1N1P1			
V17	a	P2N1P1		c	ON2O			
	b	P1N2O	V30	a	P2OP1			
V18	a	P2N1O		b	P1N1O			
	b	P1N2N1		c	ON2N1			

$$\begin{cases} 4i_{c1} = -(3F_{17} + 2(F_{11}^b + F_{10}^b) + F_{18})i_1 - (3F_{27} + 2(F_{21}^b + F_{20}^b) + F_{28})i_2 \\ -(3F_{37} + 2(F_{31}^b + F_{30}^b) + F_{38})i_3 \\ 4i_{c2} = (F_{17} - F_{18} - 2(F_{11}^b + F_{10}^b))i_1 + (F_{27} - F_{28} - 2(F_{21}^b + F_{20}^b))i_2 \\ +(F_{37} - F_{38} - 2(F_{31}^b + F_{30}^b))i_3 \\ 4i_{c3} = (F_{17} + 2(F_{11}^b + F_{10}^b) + 3F_{18})i_1 + (F_{27} + 2(F_{21}^b + F_{20}^b) + 3F_{28})i_2 \\ +(F_{37} + 2(F_{31}^b + F_{30}^b) + 3F_{38})i_3 \\ 4i_{c4} = (F_{17} - F_{18} + 2(F_{11}^b + F_{10}^b))i_1 + (F_{27} - F_{28} + 2(F_{21}^b + F_{20}^b))i_2 \\ +(F_{37} - F_{38} + 2(F_{31}^b + F_{30}^b))i_3 \end{cases} \quad (7)$$

To reduce the size of control algorithm, the second step consists in constituting vectors groups.

Group 1 : V1, V4, V7, V10, V13, V16

Group 2 : V2, V6, V8, V12, V14, V18

Group 3 : V3, V5, V9, V11, V15, V17

Group 4 : V19, V21, V23, V25, V27, V29

Group 5 : V20, V22, V24, V26, V28, V30

Group 6 : V31, V32, V33, V34, V35, V36

Third step consists in analyzing the influence of different groups of redundant vectors on capacitors voltages, under different conditions of load currents.

Fourth step consists to choice the redundancies. For each case of redundancy, the vector which tends to cancel the unbalance in capacitor voltages will be selected. In other words, we select the vector which charge the undercharged capacitors, and discharge the overcharged ones.

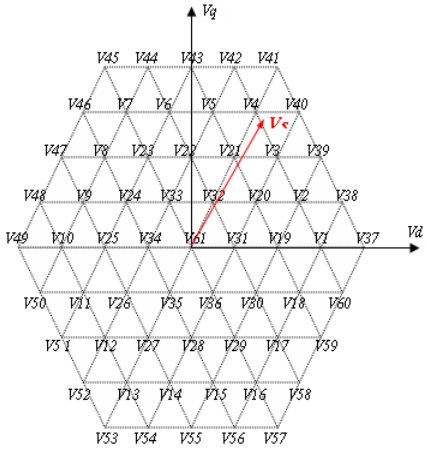

Figure 7. Space vector diagram of a five-level inverter

5 Simulation results

Simulation is divided in three times. In first time (0S<t<2S), the feedback control of the two-level rectifier is applied but the five-level VSI balancing DC bus algorithm is not used.

One remarks that the output voltage U_{cm} of two-level rectifier is equal to its reference U_{cref}=1040V (Fig. 8), but the voltages U_{c1}, U_{c2}, U_{c3} and U_{c4} are unbalanced (Fig. 9). One observes also that torque ripple of induction motor increase progressively (Fig. 10).

In second time (2S<t<7S), the five-level VSI balancing DC bus algorithm is applied. One remarks that the voltages U_{c1}, U_{c2}, U_{c3} and U_{c4} are balanced after few seconds (Fig. 9), One observes also that torque ripple decrease progressively (Fig. 10).

In third time (7S<t<10S), the nominal torque of induction motor is applied. One observe that voltages U_{c1}, U_{c2}, U_{c3} and U_{c4} are balanced and not disturbed after application of nominal torque (Fig. 9).

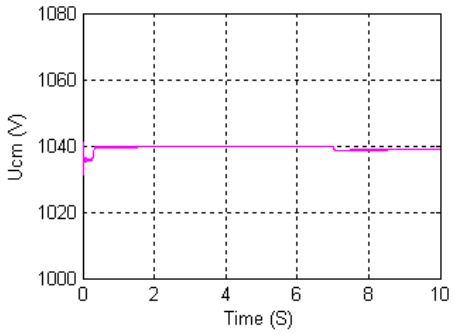

Figure 8. Output voltage of two-level rectifier

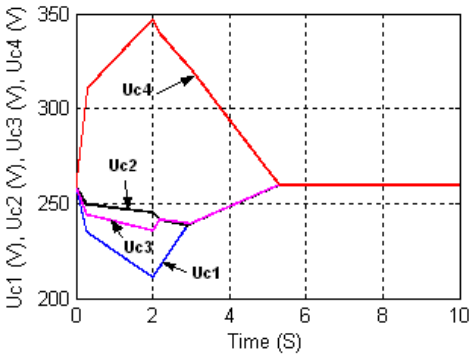

Figure 9. DC bus capacitors voltages of five-level VSI

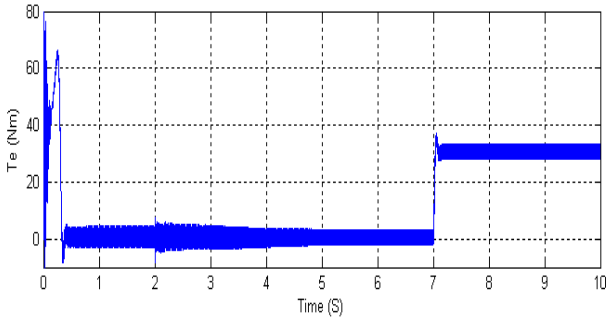

Figure 10. Induction motor torque

6 Conclusion

The present contribution intends to demonstrate that the unbalance of DC bus of back-to-back connected two-level PWM rectifier-five-level NPC VSI, causes a torque ripple in induction motor.

The proposed feedback control algorithm to the two-level rectifier associate to the space vector PWM balancing capacitor voltages of five-level NPC inverter algorithm shows a good following of the average output voltage of rectifier and the balancing of input voltages of inverter. Consequently, a torque ripple of induction motor is reduced. The proposed control algorithm opens the door to different applications of NPC multilevel converters in high power utilities such as, motor drives, doubly fed induction generators, active power filters and power supply networks interconnection.

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