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Accurate SPICE Modeling of Poly-silicon Resistor in 40nm CMOS Technology Process for Analog Circuit Simulation

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ABSTRACT: In this paper, the SPICE model of poly resistor is accurately developed based on silicon data. To describe the non-linear R-V trend, the new correlation in temperature and voltage is found in non-silicide poly-silicon resistor. A scalable model is developed on the temperature-dependent characteristics (TDC) and the temperature-dependent voltage characteristics (TDVC) from the R-V data. Besides, the parasitic capacitance between poly and substrate are extracted from real silicon structure in replacing conventional simulation data. The capacitance data are tested through using on-wafer charge-induced-injection error-free charge-based capacitance measurement (CIEF-CBCM) technique which is driven by non-overlapping clock generation circuit. All modeling test structures are designed and fabricated through using 40nm CMOS technology process. The new SPICE model of poly-silicon resistor is more accurate to silicon for analog circuit simulation.

Keywords: poly-silicon resistor; temperature-dependent voltage characteristics (TDVC); parasitic capacitance, SPICE model

1 INTRODUCTION

Poly-silicon resistor is widely used as an important device in CMOS analog circuit design [1] such as band-gap, integrator or DAC. It is necessary to use an accurate model for circuit simulation in DC and AC performance.

In the conventional way of industry, the modeling equations which include temperature-dependent characteristics (TDC) [2-3] and voltage-dependent characteristics (VDC) [4-5] are same in silicide and non-silicide poly-silicon resistor. With the CMOS technology being developed into 40nm, VDC has a secondary temperature effect only on non-silicide poly-silicon resistor. Hence, the old SPICE model equations can't meet the real silicon data. On the other hand, the accurate parasitic capacitance of poly-silicon resistor is also a key [6] in SPICE model. However, they are always traditionally simulated by field-solver. Due to some process variation such as etching [7], erosion [8] and optical proximity correction (OPC) [9], the field-solver simulation data loses accuracy without real silicon verification.

In this paper, the SPICE models of poly-silicon resistor in 40 nm technology have been optimized based on silicon data. In the section 2 and section 3, the temperature-dependent voltage characteristics (TDVC) are found to replace VDC and a novel scalable model is established with TDC and TDVC in non-silicide poly-silicon resistor. In the section 2 and section 4, the capacitance test structure is designed to extract real parasitic data using an efficient and precise on-wafer test technique from the group former work [10].

2 MODELING TEST STRUCTURE DESIGN

The topological modeling structure of three-terminal poly-silicon resistor in this paper is shown in Figure 1. R_{main} is main part resistance of poly-silicon, and C_1 and C_2 is a couple of symmetrical capacitance between poly and substrate. According to Figure 1, test structures are designed and measured to describe these components in a precise way.

2.1 *I-V test structure*

Figure 2 shows the layout of I-V test structures of both N^+ and P^+ non-silicide poly-silicon resistor corresponding to different width (W) from 0.36μm to 3.6μm and Length (L) from 4.5μm to 72.9μm. The numbers of sheet resistance is defined as L/W.

All I-V structures are designed with four terminals and they are tested by Kelvin technique [11] using Agilent B1500A under -40℃, 25℃ and 125℃. The calculation of resistance is shown in Equation 1, the step of force current is set up by 16μA and the sense voltage is limited under the range of -4V to 4V:

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$$R = \frac{V_{sence1} - V_{sense2}}{I_{force}} \quad (1)$$

2.2 *Parasitic capacitance test technique and structure*

From the group former work [10], the on-wafer capacitance test technique has been proved to be an efficient and precise way. The schematic is shown in Figure 3. The charge-induced error-free charge-based capacitance measurement (CIEF CBCM) [12] in the dashed frame is driven by non-overlapping clock generation circuit to simplify the test procedure.

The Figure 4 shows the pulse program. In step 1, V_{IN1} is input with a traditional pulse and V_{IN2} is set up to ground. In step 2, both V_{IN1} and V_{IN2} share the same pulse with step1. As a result, the system parasitic capacitance C_{par} is de-embedded. I_{step1} and I_{step2} are recorded on the pad of V_{dd} by two steps. Then C_{load} can be calculated in Equation 2, where f is the frequency of pulse and V_{dd} is the working voltage. Agilent 8110A is used to generate pulse and Agilent B1500a is used to measure the average current:

$$C_{load} = \frac{I_{step1} - I_{step2}}{V_{dd} \cdot f} \quad (2)$$

Several numbers of the poly finger are designed in parallel to compose C_{load} between poly and substrate. The layout of C_{load} is designed in Figure 5 and NF is defined as the number of Finger. To avoid apparent non-linear effects of I-V, silicide poly-silicon resistor is chosen because of its metal-like performance and the same geometry structure with non-silicide poly-silicon resistor. In Figure 5, L is fixed in 15μm, W changes from 0.36μm to 1.8μm. The whole layout of on-wafer test technique with poly structure is shown in Figure 6. The layout occupies only 40μm×70μm area.

All Kelvin R-V test structures and CBCM capacitance test structure with C_{load} are fabricated through using 40nm LP CMOS technology. And then in the next two sections, all silicon data are from on-wafer measurement on Cascade probe station.

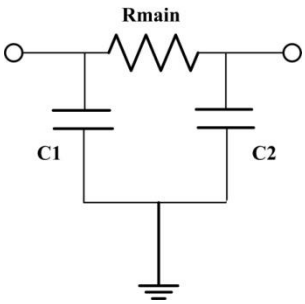

Figure 1. Topological structure of three-terminal poly resistor.

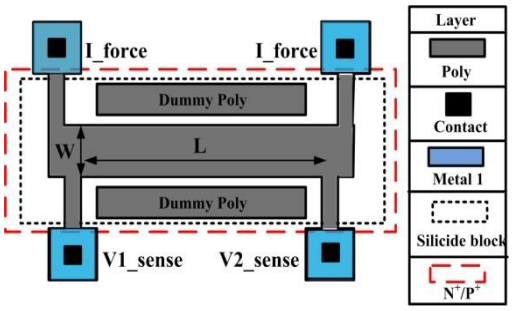

Figure 2. Layout of Kelvin test structure of non-silicide poly-silicon resistor.

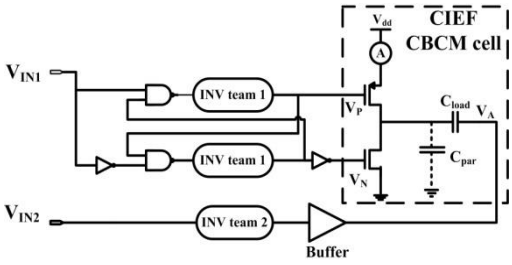

Figure 3. Schematic of the on-wafer capacitance technique

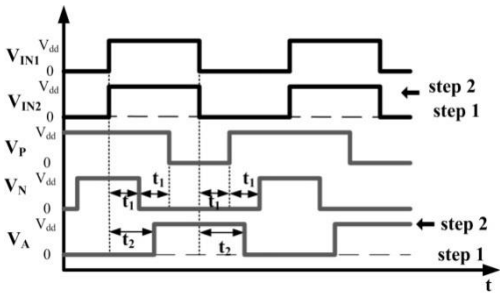

Figure 4. Input and output of pulse program by non-overlapping clock generation circuit.

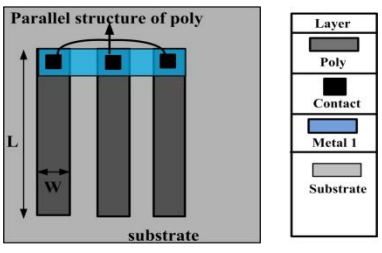

Figure 5. Layout of capacitance test structure of poly in parallel.

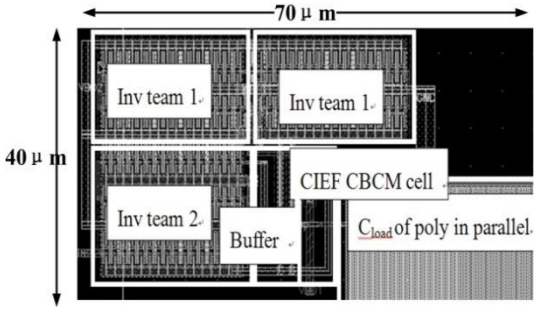

Figure 6. Whole layout of test structure in Cadence Virtuoso.

3 R-V MODELING FLOW

Based on Equation 1, R-V data is transferred from I-V data. Figure 7 shows the R-V data of P^+ non-silicide poly-silicon resistor V.S. old model simulation. When the poly sizes get smaller, the R-V curves under different temperature show the larger difference in curvature. VDC is influenced by temperature more and more serious in sub-nano CMOS process. The old model format which is same as the metal-performance-like silicide poly-silicon resistor can't meet the new global effect TDVC in Figure 7. A new scalable modeling flow based on silicon data is set up as shown in the following steps.

3.1 *Step 1: R_0 modeling*

R_0 is defined as the 0V resistance under 25℃. The formula of R_0 is shown in Equation 3, where *rsh* is sheet resistivity, *dl* and *dw* is the correction between real size and design size in on side:

$$R_0 = rsh \cdot \frac{L - 2 \cdot dl}{W - 2 \cdot dw} \tag{3}$$

Figure 8 shows the fitting result of R_0 modeling of all geometry size, where the dots are silicon data and the solid lines are model simulation.

3.2 *Step 2: TDC modeling*

R_{T0} in Equation 4 is defined as the temperature-dependent R_0. In Equation 5, TDC coefficient *tcoeff* is composed of the first-order modeling parameter *tc1r* and second-order modeling parameter *tc2r*. DTEMP is the difference between 25℃ and test temperature. In Equation 6 and Equation 7, *tc1r* and *tc2r* are both scalable with W, where *tw*, *to*, *tww* and *too* are fitting parameters.

$$R_{T0} = R_0 \cdot tcoeff \tag{4}$$

$$tcoeff = 1 + DTEMP \cdot (tc1r + tc2r \cdot DTEMP) \tag{5}$$

$$tc1r = tw \cdot W + to \tag{6}$$

$$tc2r = tww \cdot W + too \tag{7}$$

The fitting result of TDC modeling in four nominal geometry sizes is shown in Figure 9.

3.3 *Step 3: TDVC modeling*

To describe the TDVC on silicon data, Voltage-dependent coefficient *vcoeff* in Equation 8 and Equation 9 not only considers the scale influence of W and N, but also should include temperature factor DTEMP. With the poly size getting smaller in Figure 5, TDVC becomes more and more serious, so TDVC modeling parameter *tvcr* is scalable with W to describe this global effect in Equation 10. In TDVC modeling process, *vco*, *vcw*, *vcn*, *tvw* and *tvo* are fitting parameters:

$$R = R_{T0} \cdot [1 + vcoeff \cdot (\frac{V}{L})^2] \tag{8}$$

$$vcoeff = (vco + vcw \cdot W + vcn \cdot N) \cdot (1 + tvcr \cdot DTEMP) \tag{9}$$

$$tvcr = tvw \cdot W + tvo \tag{10}$$

The fitting result of TDVC modeling in P^+/N^+ non-silicide poly-silicon resistor is shown in Figure 10. All silicon data and simulation are normalized by R_{T0} to make the fitting result clearly. The simulation result from new model considered with TDVC is much better than old model. In Table 1, all obtained fitting parameters in the whole modeling flow are summarized by P^+ and N^+ non-slicide poly-silicon resistor.

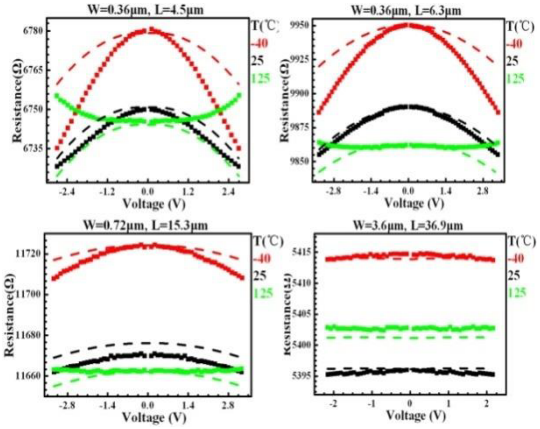

Figure 7. R-V data of P^+ non-silicide poly-silicon resistor V.S. old model. The dots are silicon data and the dashed lines are from old model simulation.

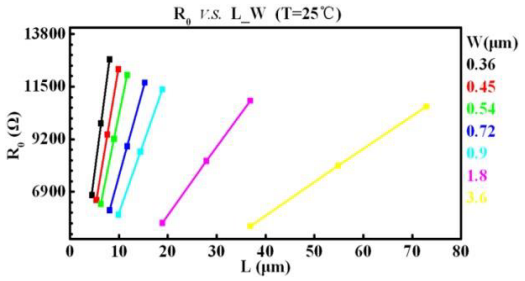

Figure 8. R_0 modeling of P^+ non-silicide poly-silicon resistor with all W and L. The dots are silicon data and the solid lines are new model simulation.

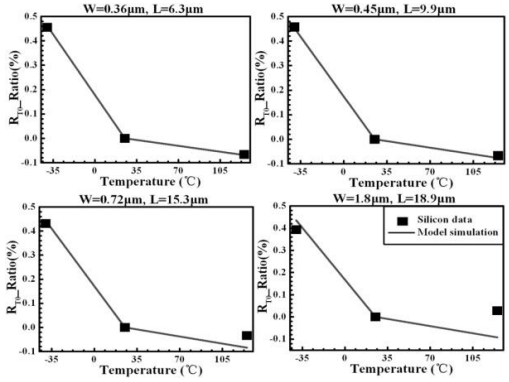

Figure 9. TDC modeling fitting of P^+ non-silicide poly-silicon resistor in four nominal sizes. The dots are silicon data and the solid lines are new model simulation.

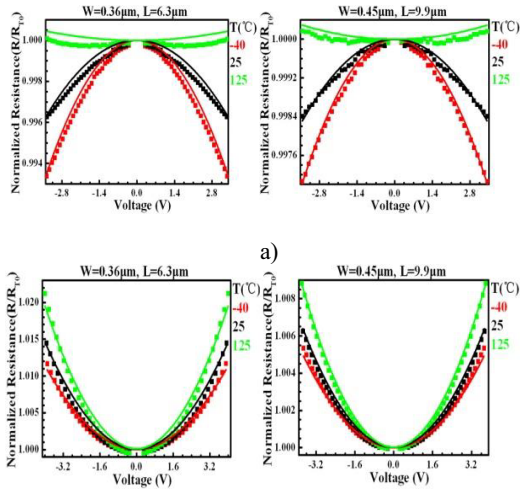

Figure 10. TDVC modeling in nominal size. The dots are silicon data and the solid lines are new model simulation, and all data are normalized by R_{T0}. (a) P^+ non-silicide poly-silicon resistor. (b) N^+ non-silicide poly-silicon resistor.

Table 1. Summary of model fitting parameters in non-silicide poly-silicon resistor

Parameters	Value	
	P^+ poly	N^+ poly
rsh [Ω/sq]	522	192.7
dl [μm]	0.122	0.043
dw[μm]	0.019	0.027
tw [1/(μm·℃)]	2.898×10^{-6}	2.723×10^{-6}
to [1/℃]	-4.68×10^{-5}	-1.11×10^{-5}
tww [1/(μm·℃²)]	-7.236×10^{-8}	5.339×10^{-8}
too [1/℃²]	4.15×10^{-7}	6.34×10^{-8}
vco [μm²/V²]	-5.77×10^{-3}	6.95×10^{-3}
vcw [μm/V²]	-5.28×10^{-3}	0.098
vcn [μm²/(V²·sq)]	-2.38×10^{-4}	1.282×10^{-3}
tvw [1/(μm·℃)]	-3.863×10^{-3}	-2.587×10^{-4}
tv0 [1/℃]	-1.05×10^{-2}	3.577×10^{-3}

4 PARASITIC CAPACITANCE EXTRACTION FLOW

4.1 *Conventional method of extraction*

The poly-silicon resistor structure is shown in Figure 11 with its parasitic capacitance to the substrate in one-side. The vertical overlap capacitance (C_{ov}) between the bottom of poly to the substrate, the fringing capacitance between the L-direction (C_{fL}) and W-direction (C_{fW}) sidewall of poly to the substrate are all considered to be extracted.

In the conventional way in the industry, the parasitic capacitance of poly-silicon resistor is simulated by field solver such as Synopsys Raphael without any silicon verification. However, such parasitic capacitance is deeply influenced by the geometry variation [10] in the sub-nano CMOS technology. In Figure 12, only simplified poly structure can be accepted in Raphael [13] without any variation considering, so the parasitic capacitance can't be accurate to the silicon.

4.2 *On-silicon way of extraction*

Based on the analysis of Figure 1 and Figure 11, the method of parasitic capacitance extraction is built in Equation 11. To extract the parasitic capacitance in a scalable way in Equation 12 and 13, C_{ov} are normalized to W×L in C_{ov0}, C_{fw} and C_{fl} are normalized to W and L in C_{f0}.

$$C_{total} = C_1 + C_2 = (C_{ov} + 2\cdot C_{fW} + 2\cdot C_{fL})\cdot NF \quad (11)$$

$$C_{ov0} = \frac{C_{ov}}{W \cdot L} \tag{12}$$

$$C_{f0} = \frac{C_{fW}}{W} = \frac{C_{fL}}{L} \tag{13}$$

Figure 13 shows silicon data extraction V.S. conventional Raphael simulation, and all capacitance is normalized by NF and L. From Figure 13, silicon data is smaller than simulation data about 5%~9%, the error can be considered as cause of geometry variation due to process. According to Equation 11, Equation 12 and Equation 13, C_{ov0} and C_{f0} are extracted in Table 2. All N^+/P^+ silicide and non-silicide poly-silicon resistors can share these equations and parameters in their SPICE model because they are in the same geometry structure.

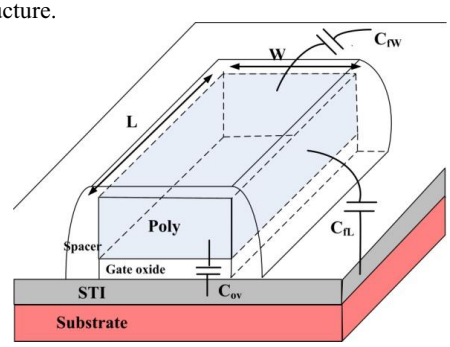

Figure 11. 3D-view of poly-silicon resistor. Its parasitic capacitance conclude C_{ov}, C_{fw} and C_{fL}.

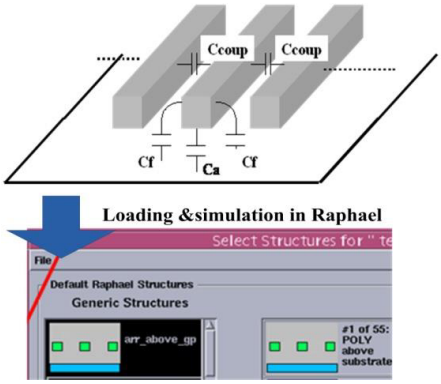

Figure 12. Traditional way to simulate the simplified poly-silicon resistor structure in Raphael.

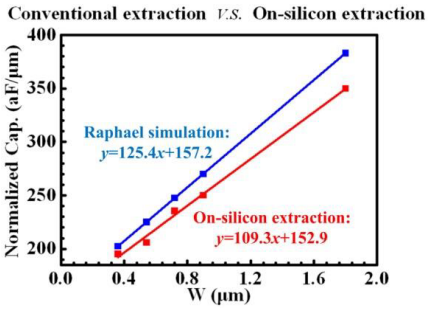

Figure 13. Parasitic capacitance extraction result of on-silicon V.S. Raphael simulation. The red dots are silicon data and the red line is on-silicon extraction model. The blue lines are Raphael simulation data and the blue line is Raphael model.

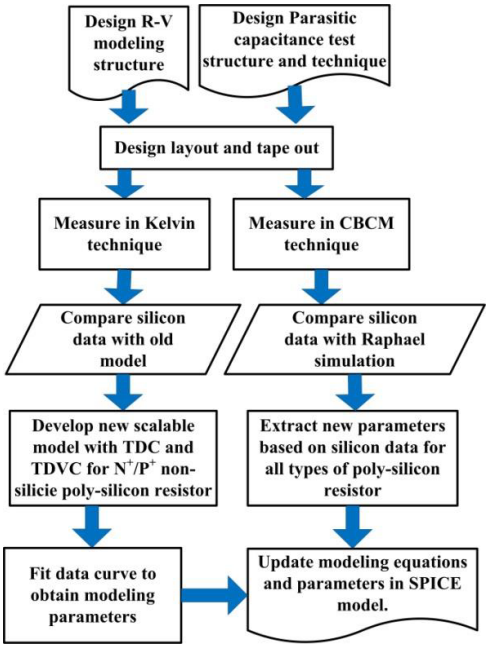

Figure 14. Total flow of R-V modeling and parasitic capacitance extraction of poly-silicon resistor in sub-nano CMOS technology.

Table 2. Summary of extraction parameters of parasitic capacitance in N^+/P^+ silicide and non-silicide poly-silicon resistor

Parameters	Value
C_{ov0} [aF/μm^2]	99.11
C_{f0}[aF/μm]	76.45

5 CONCLUSION

In this paper, a complete on-silicon modeling flow has been developed. Figure 14 has summarized the whole flow from test design to measurement and modeling. A new SPICE model with novel TDVC and silicon-based parasitic capacitance is updated for 40nm CMOS technology analog circuit simulation design. Compared with conventional model in R-V and parasitic capacitance, the new one is much nearer to silicon and can fit data better.

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