

DualBLESS: Bufferless Router with Dual Ejection Ports for 2D and 3D NoC

Chaoyun Yao*, Chaochao Feng & Mingxuan Zhang
School of Computer, National University of Defense Technology, Changsha, Hunan, China

Shaojun Wei
The Department of Electronic Systems, Tsinghua University, Beijing, China

ABSTRACT: In this paper, the authors proposed a 1-cycle bufferless router with dual ejection ports (which is also called DualBLESS) for 2D and 3D Network-on-Chip. The router uses a simple route computer module, a MUX module instead of the Flit Ejector module and a MUX module in a baseline bufferless router to achieve high performance. Simulation results under six synthetic workloads illustrate that the two proposed DualBLESS routers achieve less average packet latency and higher throughput than the baseline 2D and 3D bufferless routers.

Keywords: DualBLESS ;bufferless router; Dual Ejection Ports

1 INTRODUCTION

As the transistors continue to scale with Moore's law, the number of cores on a single chip continues to increase in order to utilize the transistors efficiently. Network-on-Chip (NoC) was shown to be feasible and easy to scale for supporting a large number of cores [1].

Previous on-chip network designs commonly assumed that each router in the network contains buffers to store the packets which are transmitted within the network. Though buffers can improve the network bandwidth utilization rate and reduce the packet lost and misroute rate, it has some shortcomings: buffers take up a significant fraction of NoC power [2] and area [3]. Thus, the bufferless NoC designs have come forth, and a few recent work have been investigated how to eliminate the in-router buffers [4, 5]. Bufferless router only contains pipeline registers, so it can reduce power and area of router significantly. The bufferless router can be separated into two classes: the drop-based router [5] and the deflection-based router [6,7]. The drop-based bufferless router needs additional logic to deal with dropped packets, which increases hardware cost. In deflection-based bufferless router and packets are deflected to another output port if an output port which has the lowest distance to the destination node is not available. It needs to avoid livelock due to the deflection routing is a non-shortest path routing algorithm. At present, the deflection routing uses packet priority to avoid livelock. However, this scheme results in a very long critical path, which limits the frequency of the router. CHIPPER [7] was proposed to eliminate the complex logic of the output port allocator. But CHIPPER router still adopts two pipelines, and introduces a complex rule to avoid

livelock. BLESS_PERM [8] is a simple 1-cycle high performance bufferless router, which uses a simple permutation network to replace the serialized allocator and switch to reduce the critical path length. However, BLESS_PERM router still has low throughput and high latency when injection rate is increased.

In this paper, we propose a 1-cycle bufferless router with dual ejection ports for 2D and 3D NoC (called DualBLESS). This router increases an additional output port at the baseline 2D and 3D router [8, 9], which can eject two flits in one cycle. DualBLESS router decreases flits deflection rate, which can decrease packet latency and improve network throughput. Experimental results indicate that in synthetic workloads, the 2D and 3D DualBLESS routers have less average packet latency than the baseline 2D and 3D bufferless routers.

The rest of paper is organized as follows. The baseline 2D and 3D bufferless routers are introduced in Section 2. Section 3 proposes the 1-cycle 2D and 3D bufferless router with dual ejection ports. In Section 4, simulation experimental results are presented, analyzed and followed by the conclusion in Section 5.

2 BASELINE BUFFERLESS ROUTER

2.1 Baseline 2D bufferless router

This paper adopts BLESS_PERM router as the baseline 2D bufferless router. The structure of the baseline 2D bufferless router is shown in Figure 1.

This router works as follows: The flit ejector judges whether input flits arrive at the destination node or not. If the destination of the flit is the current node, the flit ejector produces the selection signal of the 4-to-1

*Corresponding author: ycy021417@163.com

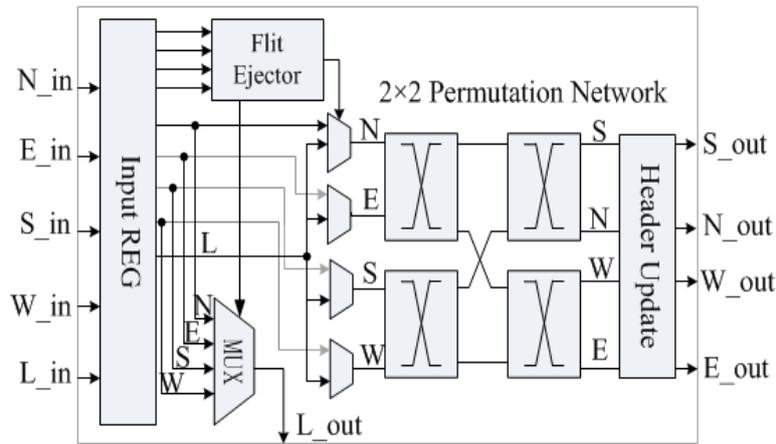


Figure 1. Baseline 2D bufferless router

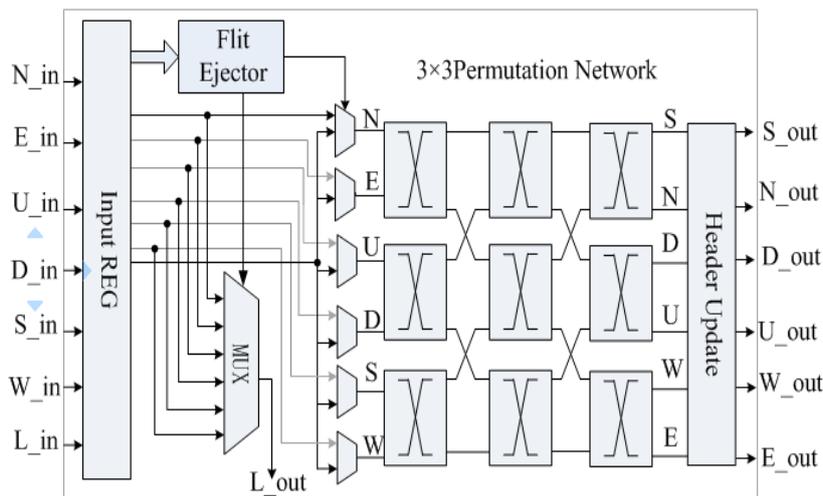


Figure 2. Baseline 3D bufferless router

multiplexer. The ejector also judges whether the local node can inject a flit or not. If the number of input flits is less than 4, the local node can inject a flit. The permutation network of the router includes two stages. Each stage includes two 2*2 permutation cells. In the case of two flits contending for the same output of the permutation cell, the permutation cell selects the flit with the higher priority to the shortest output port and misroutes the other flit to the other output. When two or more flits arrive at the destination node at the same time, the 4-to-1 multiplexer only selects one flit to the destination node and misroutes other flits, which increases flit latency and reduces the throughput. Therefore, it is necessary to redesign the router to make it accept multi-flits at the same node in a cycle to improve performance of the router.

2.2 Baseline 3D bufferless router

The baseline 3D bufferless router is a 1-cycle router with a 3-stage permutation network [9]. The structure of the baseline 3D bufferless router is shown in Figure 2. This router works similarly as the baseline 2D bufferless router. The difference is that the 4-to-1 multiplexer is replaced as the 6-to-1 multiplexer and the permutation network contains 3 stages.

3 DUALBLESS ROUTER

3.1 DualBLESS router for 2D NoC

Although the BLESS_PERM router can enhance the performance of the bufferless router, it can only eject

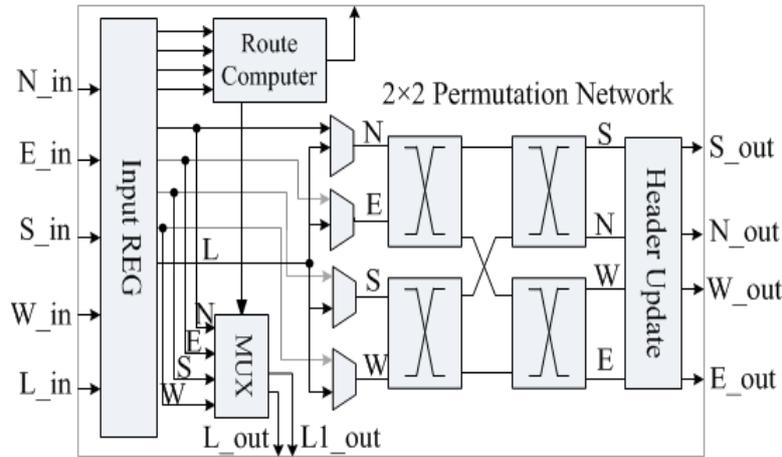


Figure 3. DualBLESS router with two output ports

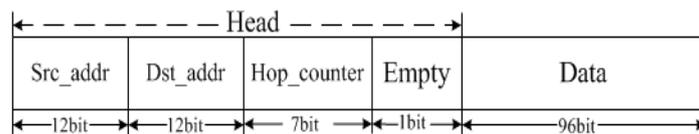


Figure 4. Flit format

one flit in a cycle, which increases the average packet latency and reduces the throughput of the network. We modify the flit ejector and the 4-to-1 multiplexer to propose a DualBLESS router with two ejection ports, which can eject two flits in a cycle. The structure of the DualBLESS router is shown in Figure 3. The router adopts the deflection routing which means the packet are not stored in the buffer of the router. When the router injects a flit, it immediately transmits it to the next router. Each flit has 128 bits. The structure of the flit is shown in Figure 4. The header of the flit has 32 bits, the data of the flit has 96 bits. There are four fields in the header of the flit. Both destination address and source address adopt relative address. In the address field, six bits are the row address and the other six bits are the column address. Hop counter with seven bits records the number of hops and the flit going through the network. The flit which has larger hop counts can be routed to its desired port. When a flit goes through a router, both address fields and hop counts field are updated in the Header Update module in Figure 3. The empty bit in the flit shows whether the flit is valid or not. Each flit of the packet contains a header field which can be independently routed in the network and arrive at the destination out of order. Therefore, it needs a reassemble buffer in the destination node to reorder the arriving packet.

Due to the fact that the flit is not buffered in the router, the deflection routing algorithm is deadlock-free. When the shortest port is occupied by

the other flit, the flit will be deflected to the other port and far away from the destination node, which may produce livelock so that the flit will never arrive at the destination. Thus it is necessary to restrict the deflection to avoid livelock. Permutation cell will compute the shortest path port according to the destination addresses of two flits. The flit with larger hop counts will be routed through the shortest path port, and the other flit will be deflected to the other port. Two stage permutation cells guaranteeing the higher priority flit will be routed through the shortest path port, which can avoid livelock.

In Figure 3, the Route Computer module judges how many flits arrive at the destination. If only one flit arrives at the destination node, the Route Computer module will produce the selecting signals of the MUX model. If one more flits arrive at the destination node, the Route Computer model will judge two flits that have larger hop counts than other flits and produces another selecting signals of the MUX model. The MUX model accepts signals from the Router Computer module to eject one or two flits in a cycle. The work flow of the MUX model is shown in Figure 5 .

The Route Computer module also decides whether the local node can inject a flit to network or not. If the number of input flits is less than four, the local node can inject a flit to the empty input port of the permutation cell. The order of output ports of the permutation cells is South, North, West, and East,

while the order of input ports of the permutation cells is North, East, South, and West. The corresponding order can avoid the input flit which reflects back to the same input direction which can decrease the deflection rate.

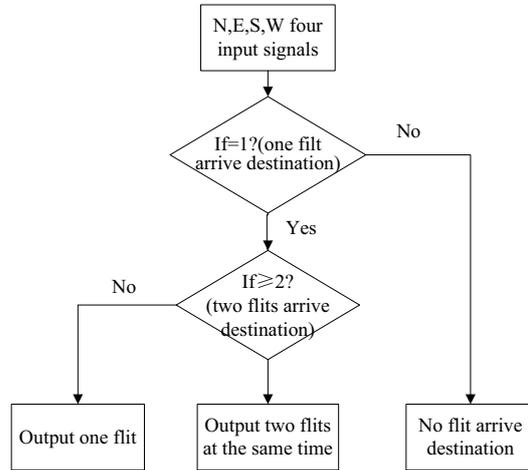


Figure 5. MUX module output scheme

3.2 DualBELSS router for 3D NoC

Although the bufferless router with the permutation network can enhance the clock frequency of the baseline 3D bufferless router, the router can only eject one flit in a cycle. The router in the center of the network may have six flits come to the destination node at the same time. This router can only eject one flit in a cycle which makes too many flits to deflect far away from the destination node. It may increase the latency of the flit and easy to cause the network in saturation status. Therefore, we redesign the flit reject module and the multiplexer to increase a flit ejection port, which can eject two flits in a cycle. The structure of the 3D DualBLESS router with two ejection ports is shown in Figure 6. This router works similarly as the 2D DualBLESS router.

4 PERFORMANCE EVALUATION

4.1 Experiment results for 2D router

We evaluate the performance of two DualBELSS routers using a cycle-accurate NoC simulator which is developed in VHDL under six synthetic workloads. The simulations are performed on an 8*8 2D mesh. Each packet contains 4 flits. For synthetic workloads, we use four traffic patterns: uniform random, transpose, bit complement and bit reverse. We measure throughput and average packet latency in the experiment. The throughput of the network is defined as the saturation point of the network which means the

maximum accepted traffic. The formula is shown as follows:

$$\text{Throughput} = \frac{N_{\text{total_received_flits}}}{N_{\text{nodes}} \cdot T_{\text{measure_time}}}$$

The unit of throughput is flits/cycle/node, where $N_{\text{total_received_flits}}$ represents the total received flits of all nodes in the network, N_{nodes} is the number of nodes in the network and $T_{\text{measure_time}}$ is the total measurement time in the simulation.

The packet latency is defined as the time between the source node which produces the first flit and the destination node which receives the last flit. The latency includes the flit waiting in the buffer queue before injecting into the network. The formula of the average packet latency is shown as follows:

$$\text{AverageLatency} = \frac{\text{TotalLatency}}{N_{\text{total_packets}}}$$

Figure 7 shows the throughput of the two routers with six synthetic workloads. Compared with the 2D BASEBLESS router, the 2D DUALBLESS router respectively achieves more throughput of 7.7%, 2.9%, 7.2%, 4.2%, 9.4% and 3.2%.

Figures 8(a)-(f) respectively show the average packet latency of two bufferless routers with six synthetic workloads. Compared with the BASEBLESS router, the DUALBLESS router respectively achieves 19.4%, 26.1%, 21.7%, 62.3%, 49.8% and 26.7% less average packet latency. When the injection rate is close to saturation, the DUALBLESS router respectively achieves less average packet latency of 86.1%, 52.9%, 57.1%, 76.8%, 69.2% and 36.8%.

4.2 Experiment result for 3D DualBELSS router

We evaluate the performance of two 3D bufferless routers using a cycle-accurate NoC simulator which is developed in VHDL under synthetic workloads. The simulations are performed on a 4*4*4 3D mesh network. Each packet contains 4 flits. We use six traffic synthetic patterns: uniform random, transpose, bit complement, bit reverse, shuffle and tornado. Other configurations are the same as the 2D DualBLESS router. We measure throughput and average packet latency in the experiment.

Figure 9 shows the throughput of the network with two 3D bufferless routers under six synthetic workloads. Compared with the BASEBLESS router, the DUALBLESS router respectively achieves more throughput of 16%, 3.5%, 3.6%, 12.5%, 10.1% and 8%.

Figures 10(a)-(f) respectively show the average packet latency of two bufferless routers with six synthetic workloads. Compared with the BASEBLESS router, the DUALBLESS router respectively achieves less average packet latency of 87.9%, 14.5%, 15.7%, 65%, 27.9% and 49%. When the injection rate is close to saturation, the DUALBLESS router respectively achieves less

average packet latency of 96.3%, 25.5%, 26.6%,
88.8%, 84.3% and 61.9%.

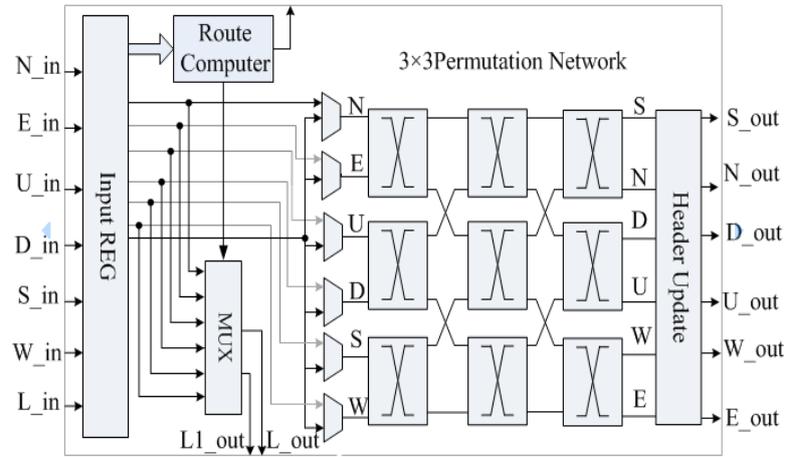


Figure 6. 3D DualBLESS router with two output ports

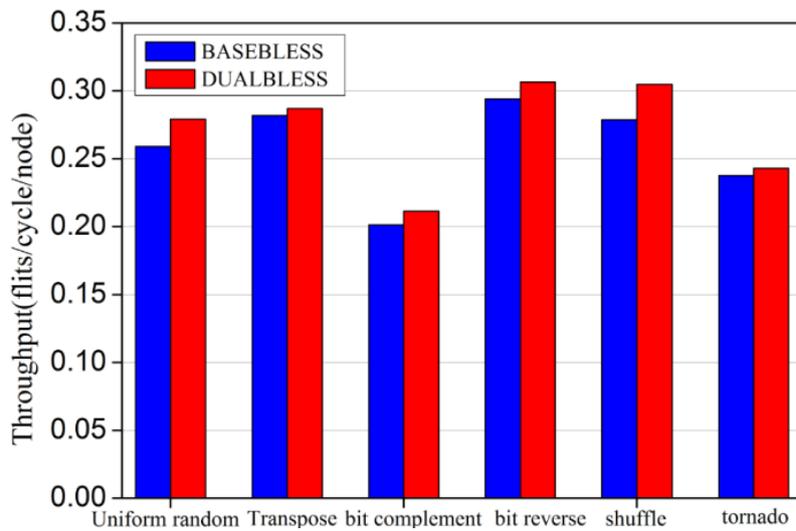
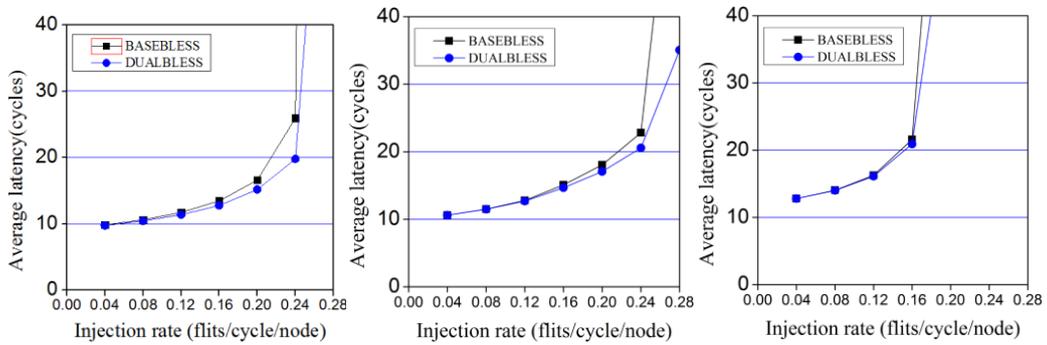


Figure 7. Throughput with synthetic workloads



(a) Uniform random

(b) transpose

(c) Bit complement

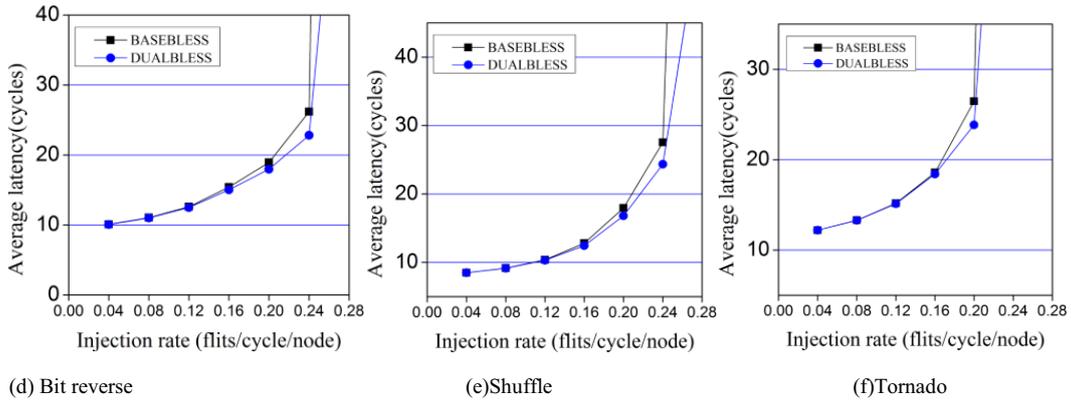


Figure 8. Average packet latency for 2D DualBLESS router

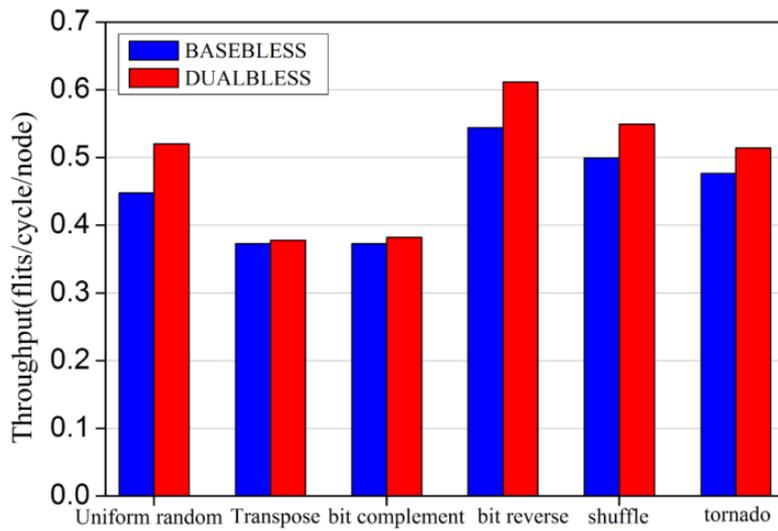
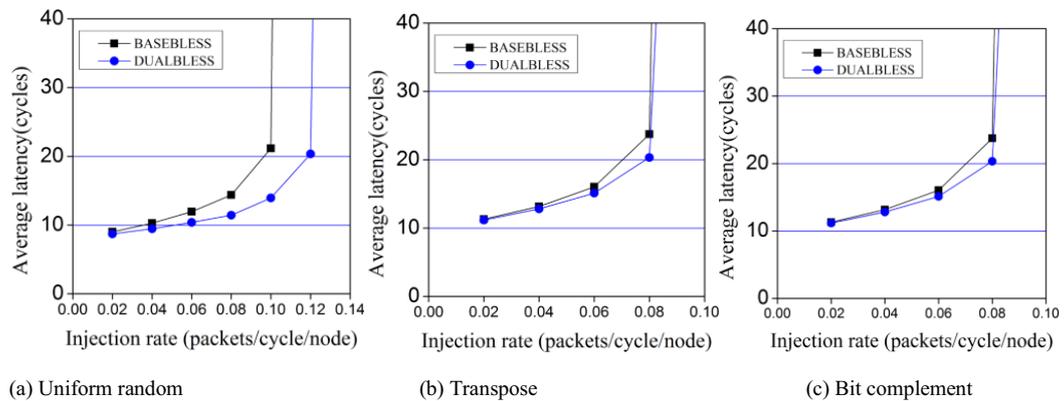


Figure 9. Throughput for 3D DualBLESS router



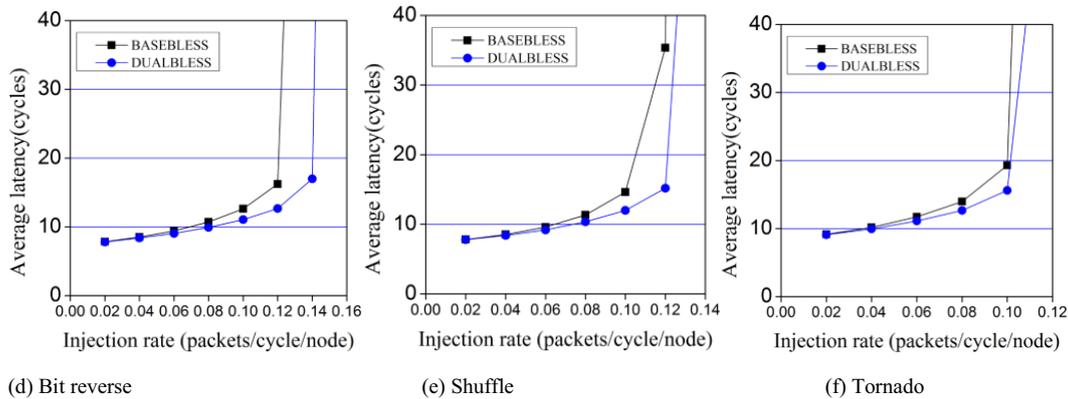


Figure 10. Average packet latency for 3D DualBLESS router

5 CONCLUSION

In this paper, we propose a 1-cycle high-performance bufferless router with dual ejection ports for 2D and 3D NoC. The router used a simple route compute module and MUX module instead of the Flit Ejector module in BASEBLESS router to achieve high performance. Compared with the baseline 2D/3D router, the proposed router can achieve less packet latency and higher throughput.

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REFERENCES

- [1] W. J. Dally and B. Towles. 2001. Route packets, not wires: on-chip interconnection networks. In Design Automation Conference (DAC), pp: 684-689.
- [2] Y Hoskote, S Vangal, A Singh, N Borkar, S Borkar. 2007. A 5-GHz mesh interconnect for a teraflops processor. IEEE Micro.
- [3] P. Gratz, C. Kim, R. McDonald, and S. Keckler. 2006. Implementation and evaluation of on-chip network architectures. ICCD.
- [4] Hayenga M, Jerger N E, Lipasti M. 2009. SCARAB: a Single Cycle Adaptive Routing and Bufferless Network. In Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture, pp: 244-254.
- [5] Gomez C, Gomez M E, Lopez P, et al. 2008. Reducing Packet Dropping in a Bufferless NoC. In Proceedings of the 14th International Euro-Par Conference on Parallel Processing, pp: 899-909.
- [6] Moscibroda T, Mutlu O. 2009. A Case for Bufferless Routing in Onchip Networks. In Proceedings of the 36th Annual International Symposium on Computer Architecture, pp: 196-207.
- [7] Fallin C, Craik C, Mutlu O. 2011. CHIPPER: a Low-complexity Bufferless Deflection Router. In Proceedings of the 17th IEEE International Symposium on High Performance Computer Architecture, pp: 144-155.
- [8] Feng Chao-chao, Lu Zhonghai, Zhang Minxuan and Li Jinwen. 2011. A 1-cycle 2GHz Bufferless Router for Network-on-Chip. Journal of National University of Defense Technology. 33(6): 42-47.
- [9] Chaochao Feng, Zhonghai Lu, Axel Jantsch, Minxuan Zhang. 2012. A 1-Cycle 1.25 GHz Bufferless Router for 3D Networks-on-Chip. *IEICE Transactions on Information and Systems*. E95-D(5): 1519-1522.