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Stability analysis of a high-step-Up DC grid-connected two-stage boost DC-DC converter

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Abstract. High conversion ratio switching converters are used whenever there is a need to step-up dc source voltage level to a much higher output dc voltage level such as in photovoltaic systems, telecommunications and in some medical applications. A simple solution for achieving this high conversion ratio is by cascading different stages of dc-dc boost converters. The individual converters in such a cascaded system are usually designed separately applying classical design criteria. However these criteria may not be applicable for the complete cascaded system . This paper first presents a glimpse on the bifurcation behavior that a cascade connection of two boost converters can exhibit. It is shown that the desired periodic orbit can undergo period doubling leading to subharmonic oscillations and chaotic regimes. Then, in order to simplify the analysis the second stage is considered as constant current sink and design-oriented analysis is carried out to obtain stability boundaries in the parameter space by taking into account slope interactions between the state variables in the two-different stages.

1 Introduction

Power electronics systems are present in any application where there is a need to convert a form of electrical energy into another. Examples include power supplies in consumer electronics, industrial electric motor drives, electroheating, lighting and energy-efficient interfaces between renewable energy resources and the distribution grid. These systems make use of semiconductor switching components operating at a high switching frequency to reach the desired system response at a much slower time-scale than the switching time-scale. The switch-mode operation is forced by suitable pulse width modulation (PWM) schemes applied to the main switches of the system and in practice, the desired behavior is a periodic orbit with the same period of the sampling PWM period T which is in turn equal to that of an external clock signal.

One of the most used topology is the boost converter which play a major role in many industrial applications and it is necessary whenever it is required to step-up a source voltage to a higher voltage level [1]. In many applications, a high step-up conversion ratio is needed. This is the case of, among others, uninterrupted power supplies (UPS), automobile high intensity discharge headlamps, and in some medical equipments. This is also the case of renewable energy applications such as distributed photovoltaic (PV) generation systems, fuel cell energy conversion systems and modern electrical vehicles. In these applications, although a simple boost converter can be normally used, there are many inconveniences with its use for high step-up ratio mainly related to increased stress in the components and the system efficiency. First, the voltage stress of the main switch is equal to the high output voltage, hence, a high-voltage rating switch with high on resistance should be used, generating high conduction losses. Second, high conversion ratio implies working with very high, some times prohibitive, values of duty cycles which would results in large conduction losses on the power device and this seriously decreases the system efficiency [1]. As a result, the conventional boost converter is substituted with a high conversion ratio boost converters that could work with relatively low values of duty cycle. Although there are many different topologies that can carry out successfully this task, the system consisting of cascading two simple converters remain the most natural and efficient solution for this kind of applications. For instance, in the future power grid, not only the utilities, but also the users can produce electric energy by aggregating distributed generation sources. In that context, renewable energy sources such as photovoltaic (PV) arrays will be used to feed a main (dc or ac) bus. The problem is that the renewable energy sources generate voltage levels much lower than the grid voltage. Therefore cascaded schemes are necessary in this case. Moreover, in these kind of applications, storage elements such as batteries are connected to the dc bus through DC-DC converters for ensuring an autonomous energy supply. Figure 1 shows an example of a PV power system used in combination with bi-directional DC-DC converter and a back-up battery.

Modeling and simulation methods and stability analysis are indispensable for the design of these converters. A trade off always exists between simplicity and accuracy of

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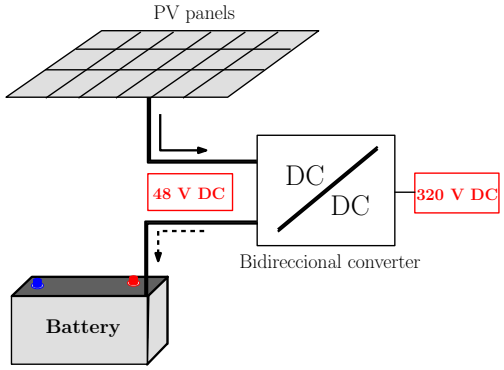


Fig. 1. Photovoltaic power system connected to a dc grid through a bidirectional dc-dc converter with a back-up battery.

the models. A model must be so simple to allow design-oriented analysis of the dynamical behavior and the same time not so simple that details of the system behavior are lost.

The desired behavior of this switching systems is a periodic orbit with the same period as the PWM sampling period. However, due to difference in time scales and nonlinearities, it is possible that the system behaves with a periodic orbit with a period equal to a multiple integer of the sampling period [2]. The system can even enter through different bifurcation scenarios into quasi-periodic or chaotic regimes. During the last couple of decades, much effort has been devoted to the study of nonlinear behavior in switching converters [2]. A large variety of complex nonlinear instability phenomena, such as period doubling leading to subharmonic oscillations, and Hopf or Neimark-Sacker bifurcations leading to slow-scale instabilities or saddle-node bifurcation leading to jump phenomenon between different steady-state solutions have been reported in switched-mode DC-DC converters. These studies, which are mostly based on accurate approaches coping with nonlinear behavior such as discrete-time mappings [3] or the Floquet theory together with *Filippov's method* [4]. These phenomena can have harmful effects on the system operation and may cause system failure, malfunctioning or even damages caused by the increase of the stress on the switching components which would rise the working temperature and this in turn would shorten the lifetime of the system. Therefore their study and prediction are important from both a theoretical and a practical points of view.

In this paper, the bifurcation behavior of two cascaded boost converters connected to a dc bus with a conversion ratio of about 6.5 is studied. The rest of this work is organized as follows: Section 2 deals with the description of the system under study. In Section 3, some bifurcation phenomena exhibited by the system are shown. Design-oriented modeling of the system is addressed in Section 4. From a reduced-order model, stability boundaries in parameter space are obtained. Design-oriented stability conditions are obtained in Section 5 where slopes interaction are revealed. Finally, some concluding remarks are drawn in the last section.

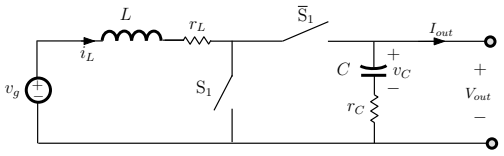


Fig. 2. Bidirectional boost dc-dc converter.

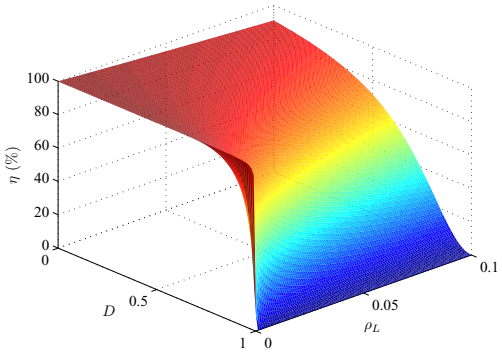


Fig. 3. The efficiency of the single stage boost converter as a function of the duty cycle D and the coefficient ρ_L.

2 High Conversion Ratio Problems and Solutions

The boost converter is shown in Fig. 2. This is a well-known switching power converter able to produce a dc output voltage larger than its input dc voltage. It step-up the input voltage v_g to a desired output voltage $v_o > v_g$ with a suitable switching of the switch. Taking into account the switching and the magnetic components losses, the conversion ratio for a single boost converter will be given by [1]

$$M(D) = \frac{\eta(D)}{1-D} \tag{1}$$

where D is the duty cycle and η is the efficiency given by

$$\eta(D) = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{1}{1+\ell} \tag{2}$$

where

$$\ell = \frac{(r_L + Dr_{DS})I_{\text{out}}}{(1-D)^2 V_{\text{out}}} + \frac{(r_{DS} + Dr_C)I_{\text{out}}}{(1-D)V_{\text{out}}} \tag{3}$$

r_L is the inductance equivalent series resistance (ESR), r_{DS} is the MOSFET on resistance, r_C is the ESR of the output capacitor and I_{out} and V_{out} are the output current and input current of the converter. For simplicity let us consider ideal switches and only losses in the energy storage elements will be taken into account. Let us also neglect the switching losses. Figure 3 shows the plot of the efficiency η as a function of the duty cycle D and the ratio $\rho_L = r_L I_{\text{out}}/V_{\text{out}}$. It can be noted that the efficiency is highly degraded for high values of the duty cycle. This justifies the use of a cascade connection of boost converters to avoid using high values of duty cycles.

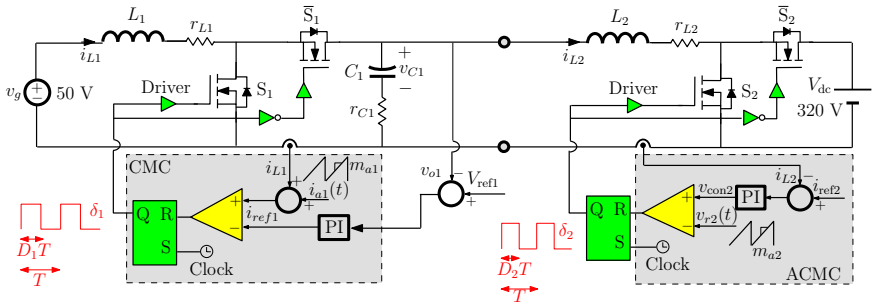


Fig. 4. Schematic circuit diagram of a boost switching converter loaded by another boost switching converter. The first stage is under a PCMC with its output voltage loop closed. The average input current in the second stage is tightly regulated by PI compensator

3 Current mode controlled cascaded boost-boost converters

3.1 System description

The two-stage dc-dc converter considered in this study is shown in Fig. 4. It consists of a cascade connection of two boost converters. It is assumed that both converter stages operate in Continuous Conduction Mode (CCM). In this case, the inductor currents i_{L1} and i_{L2} never drop to zero. The switches are considered ideal and the Equivalent Series Resistances (ESRs) of inductors and capacitors are included in the model of the circuit. For the boost converter, a current loop is always necessary due to its non-minimum phase nature if the feedback variable is the output voltage [1]. The system is controlled by comparing the inductor currents of the first and the second stages i_{L1} and i_{L2} with their reference values i_{ref1} and i_{ref2}. The inductor current in the first stage is controlled by a typical PCMC with an artificial $T-$periodic ramp compensator $i_{a1}(t)$ with slope m_{a1}. With the aim to regulate the intermediate voltage v_{C1} and the inductor current i_{L2} in the second stage to their desired values, the corresponding errors are processed by PI compensators. The intermediate voltage loop provides current reference for the first stage but it can also provide this reference to the second stage.

3.2 System Modeling

3.2.1 Power stage model

By applying Kirchoff's current and voltage laws to the circuit depicted in Fig. 4, the cascade connection of the two converters can be mathematically described by the following set of differential equations

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{v_g}{L_1} - \frac{r_{L1}i_{L1}}{L_1} - \frac{v_{C1} + r_{C1}(i_{L1} - i_{L2})}{L_1}(1-\delta_1) \tag{4}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{v_{C1} + r_{C1}(i_{L1}(1-\delta_1) - i_{L2})}{L_2} - \frac{r_{L2}i_{L2}}{L_2} - \frac{V_{\mathrm{dc}}}{L_2}(1-\delta_2) \tag{5}$$

$$\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = \frac{i_{L1}}{C_1}(1-\delta_1) - \frac{i_{L2}}{C_1} \tag{6}$$

where for the first stage (resp. second stage) $\delta_1 = 1$ when the switch S_1 (resp. S_2) is closed and $\delta_1 = 0$ when the switch S_1 (resp. S_2) is open. All the parameters that appear in (4)-(6) are shown in Fig. 4. v_{C1}, i_{L1}, v_{C2} and i_{L2} are the state variables of the power stage that stand for the capacitor voltages and the inductor currents in the first and the second stages respectively. The variables δ_1 and δ_2 are the binary command signals used to drive the switches S_1 and S_2 respectively, and v_g is the input voltage of the first stage. L_1, L_2, C_1 and C_2 are the inductances and the capacitances of the first and the second stages, r_{L1}, r_{L2}, r_{C1} and r_{C2} being their ESRs.

3.2.2 Controllers modeling

At the beginning of each switching cycle in the first stage, the switch S_1 is turned on. The controlled current i_{L1} increases until it reaches the signal $i_{\mathrm{ref1}} - m_{\mathrm{a1}}(t \bmod T)$, the switch S_1 is then turned off, and remains off until the next cycle begins. During this time, the switch $\overline{\mathrm{S}}_1$ is conducting. With the aim to regulate the output voltage to its desired value, the inductor current reference in the first stage is generated from an outer voltage loop PI controller whose input is the output voltage error $e_{v1} = V_{\mathrm{ref1}} - v_{o1}$, $v_{o1} = v_{C1} + r_{C1}\mathrm{d}v_{C1}/\mathrm{d}t$, whose output is i_{ref1} given by

$$i_{\mathrm{ref1}} = W_v(e_{v1} + \omega_{zv}x_3) \tag{7}$$

where $x_3 = \int e_{v1}(t)\mathrm{d}t$ is the voltage error integral. With the aim to regulate the the inductor current i_{L2} in the second stage to its desired value, the error $i_{\mathrm{ref2}} - i_{L2}$ is processed by a PI current compensator whose output is given by

$$v_{\mathrm{con2}} = W_i(e_{i2} + \omega_{zi}x_5) \tag{8}$$

where $x_5 = \int e_{i2}(t)\mathrm{d}t$ is the current error integral. During this time, the switch S_2 is switched on at the beginning of each switching period and switched off whenever v_{con2} crosses v_{r2}. The state of the switch $\overline{\mathrm{S}}_2$ is complementary to that of switch S_2. The control signal for the second stage can be written in terms of this new additional variable as $v_{\mathrm{con2}} = W_i[e_{i2} + \omega_z \int e_{i2}\mathrm{d}t]$. The integral action of the previous controllers involve new system state variables which can be selected to be either the integral of the output of these controllers or simply the integral of the errors x_3 and x_5. In this case, the extra state equations for these two variables are

$$\frac{\mathrm{d}x_3}{\mathrm{d}t} = V_{\mathrm{ref1}} - v_{o1} \tag{9}$$

$$\frac{\mathrm{d}x_5}{\mathrm{d}t} = i_{\mathrm{ref2}} - i_{L2} \tag{10}$$

The duty cycles are decided by comparing in the first stage the inductor current i_{L1} to the signal $i_{\mathrm{ref1}} - m_{\mathrm{a1}}t \bmod T$ and

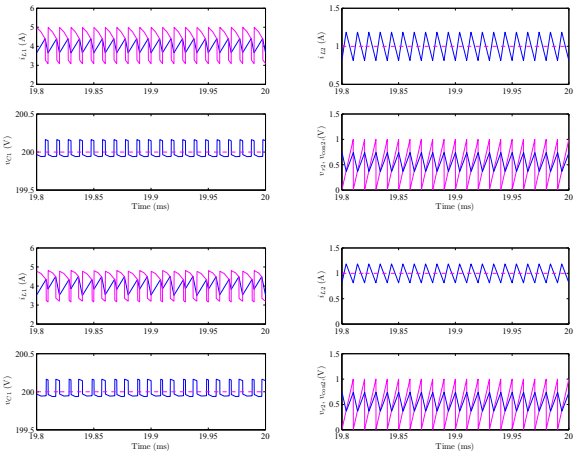


Fig. 5. Waveforms of the state variables and the control signals in the two stages. While the second stage is stable, the first stage exhibits subharmonic fast-scale instability. $C_1 = 500\ \mu$F

comparing in the second stage the control voltage v_{con2} with the $T-$periodic ramp modulator $v_{r2} = m_{\text{a2}}t \bmod T$. Therefore, the switch S_1 in the first stage is closed periodically each clock period and it is turned off whenever the following switching function

$$\sigma_1(\mathbf{x}, t) := i_{\text{ref1}} - m_{\text{a1}}(t \bmod T) \tag{11}$$

is equal to zero, where $i_{\text{ref1}} = W_v V_{\text{ref1}} + \mathbf{F}_1\mathbf{x}(t)$ is the reference current and, according to (11), the feedback vector in the first stage is $\mathbf{F}_1 = [-1,\ -W_v r_{C1},\ -W_v,\ W_v\omega_{zv},\ 0]$ and $\mathbf{x} = (i_{L1},\ i_{L2},\ v_{C1},\ x_4,\ x_5)^\top \in \mathbb{R}^5$ is the vector of state variables of the system. In the second stage the switching decision is taken by comparing the control signal $v_{\text{con2}}(t) := W_i i_{\text{ref2}} + \mathbf{F}_2\mathbf{x}(t)$ with a $T-$periodic ramp modulator $v_{r2}(t)$, where the feedback vector in the second stage is $\mathbf{F}_2 = [0,\ -W_i,\ 0,\ 0,\ W_i\omega_{zi}]$. The switching instants are therefore solutions of the following equation

$$\sigma_2(\mathbf{x}, t) := W_i i_{\text{ref2}} + \mathbf{F}_2\mathbf{x}(t) - m_{\text{a2}}(t \bmod T) = 0 \tag{12}$$

Note that $\mathbf{F}_1$ and $\mathbf{F}_2$ are also the normal vectors to the switching manifolds defined by (11) and (12) respectively. It is worth noting also that the system is linear for each switch pair state, and the nonlinearities arise in this kind of systems basically from interaction between feedback and switching processes that make the dynamics of the system highly nonlinear. For each state of the switch pair (S_1, S_2), the system can be described by a set of linear differential equations that can be written as follows $\dot{\mathbf{x}} = \mathbf{A}_{ij}\mathbf{x} + \mathbf{B}_{ij}$, $(i, j) \in \{0, 1\}^2$. Obtaining $\mathbf{A}_{ij}$ and $\mathbf{B}_{ij}$ from (4)-(6) and (9)-(10) is straightforward.

4 Bifurcation behavior

The fixed circuit parameter values used in this study are shown in Table 1 and they are selected as practical values for a connecting a PV panel whose output voltage is $v_g = 50$ V interfaced through a two-stage boost converter with a dc grid whose voltage is V_{dc}=320 V [6]. The switching frequency is $f_s = 100$ kHz. This parameter is selected equal for both stages to avoid added complexities due to possible switching frequency interaction. The intermediate voltage v_{C1} is regulated to approximately 200 V in order to make the first stage to work with a duty cycle $D_1 = 75\%$ therefore a ramp compensator is needed in this stage. The duty cycle in the second stage is $D_2 = 0.375$ and according to a classical design criterion no ramp compensation is needed. In the classical design, the minimum ramp needed to avoid subharmonic oscillations in a boost converter is given by the following expression [1]

$$\underbrace{\frac{v_o}{L}(D - \frac{1}{2})}_{m_{a,\text{cri}}(D)} < m_a \tag{13}$$

where m_a is the slope of the T-periodic artificial ramp compensator and D is the duty cycle, v_o is the output voltage and L is the inductance value. In our example, we have for the first stage $m_{a,\text{cri},1}(D_1) = v_{C1}(D_1 - 1/2)/L_1$, where $D_1 = 0.75$, *i.e,* $m_{a,\text{cri},1} \approx 119$ kA/s, being the switching frequency used $f_s = 100$ kHz, the minimum ramp amplitude must be 1.19. Therefore with a ramp amplitude equal to 1, the system must be unstable. However, we will see that this is not the case. Moreover, the minimum ramp compensator will be determined. For the second stage, the duty cycle is $D_2 = 0.375 < 0.5$ and a priori, the system can be stable even without a ramp compensator. This is the case a standalone converter. In our interconnected scheme, a ramp voltage whose amplitude is $V_{M2} = 1$ V has been used in order to avoid subharmonic oscillation at the second stage due to possible interaction with the first stage.

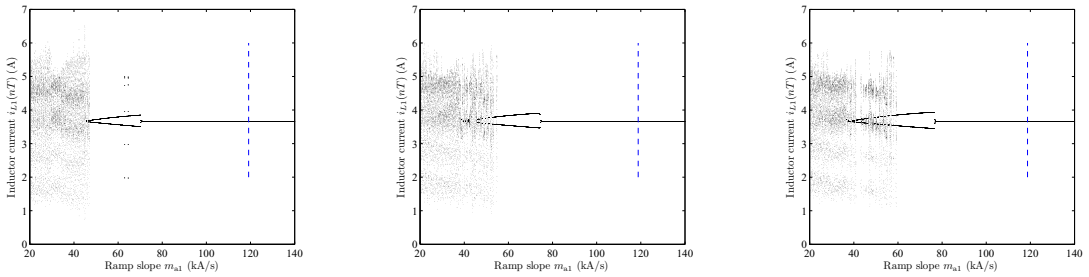
Figure 5 shows the steady-state response of the system for $m_{a1} = 100 \cdot 10^3$ A/s and $m_{a1} = 0.7 \cdot 10^3$ A/s. It can be observed that while the controlled variables are well regulated their desired values and the second stage is stable for both parameter values, the steady-state cycle-by-cycle behavior of the first stage exhibits fast-scale subharmonic oscillation for $I_{M1} = 0.7 \cdot 10^3$ A. In order to investigate further the bifurcation phenomena in the system, a bifurcation diagram is computed by taking m_{a1} as a bifurcation parameter which is varied between 0 and 25 kA/s for three values of the output capacitances C_1 =200 μF, 400 μF, 600 μF and 800 μF. The results are shown in Fig. 6. It can be observed that the larger the capacitance C_1 is, the larger the ramp slope required for stabilization is.

5 Model reduction

The inductor current i_{L2} in the second stage is programmed to track perfectly in average its reference current i_{ref2} by using a PI controller. Of course, this average current controller may fail in carrying out this task and the second stage may exhibit fast-scale subharmonic oscillation or slow-scale low frequency oscillation. Both instabilities can be avoided by selecting appropriately the ramp slope or amplitude according to a traditional design because the output voltage is constant. Under these circumstances, the average value of the inductor current in the second stage is tightly regulated in such a way that can be substituted by its reference value without losing accuracy, i.e., $\bar{i}_{L2} \approx i_{\text{ref2}}$ [5]. Therefore, the cascaded system can be approximated by the simplified scheme depicted in Fig. 7. The averaged output current in the second stage will be $i_{\text{ref2}}/M_2(D_2)$. The first stage can therefore be seen as a boost converter loaded

Table 1. The used parameter values.

L_1 r_{L1}	r_{C1}	V_{ref1}	ω_{zv}	L_2 r_{L2}	W_i	i_{ref2}	ω_{zi}
420 μH, 100 mΩ	50 mΩ	200 V	10 krad/s	2 mH, 100 mΩ	1 Ω	1 A	10 krad/s



(a) $C_1 = 400\,\mu$F (b) $C_1 = 600\,\mu$F (c) $C_1 = 800\,\mu$F

Fig. 6. Bifurcation diagram by taking m_{a1} as a bifurcation parameter for different values of C_1. Dashed vertical line stands for the stability boundary according to the traditional approach.

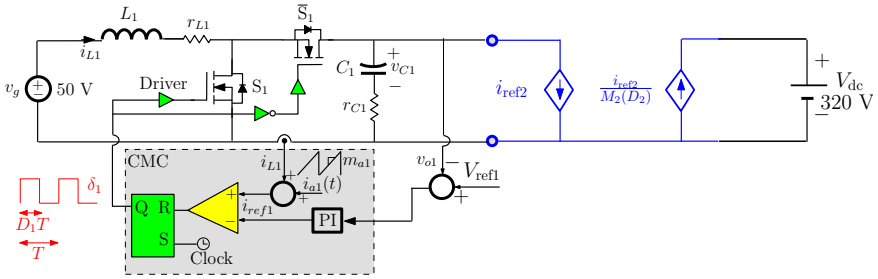


Fig. 7. Schematic diagram of the simplified system.

by a constant current sink whose dynamic behavior and its output voltage controller design has been recently addressed by state-space averaging technique [6]. However, nonlinear analysis and the bifurcation phenomena have not been reported to the author's knowledge. It is worth to note that this approximation is also valid if the second stage is another converter topology rather than the boost converter considered in this study. Note also that although a full-order model can be used to obtain numerically the critical value of the parameters, it is more useful to have a simplified reduced-order model to speed-up the simulation [5] or even to derive from it explicit analytical expressions for the stability boundaries as it will be done in the next section. The simplified system can be mathematically described by the following set of differential equations

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{v_g}{L_1} - \frac{r_{L1}i_{L1}}{L_1} - \frac{v_{C1} + r_{C1}(i_{L1} - i_{\text{ref2}})}{L_1}(1-\delta_1) \quad (14)$$

$$\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = \frac{i_{L1}}{C_1}(1-\delta_1) - \frac{i_{\text{ref2}}}{C_1} \quad (15)$$

$$\frac{\mathrm{d}x_3}{\mathrm{d}t} = V_{\text{ref1}} - v_{C1} - r_{C1}i_{L1}(1-\delta_1) + r_{C1}i_{\text{ref2}} \quad (16)$$

which can be written in matrix form as follows

$$\dot{\mathbf{x}} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{u} \quad \text{for } S_1 \text{ on} \quad (17)$$

$$\dot{\mathbf{x}} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2\mathbf{u} \quad \text{for } S_1 \text{ off} \quad (18)$$

where

$$\mathbf{A}_1 = \begin{pmatrix} \frac{-r_{L1}}{L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & -1 & 0 \end{pmatrix}, \quad \mathbf{B}_1 = \begin{pmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ 0 & r_{C1} & 1 \end{pmatrix} \quad (19)$$

$$\mathbf{A}_2 = \begin{pmatrix} \frac{-r_{L1}}{L_1} & -\frac{1}{L_1} & 0 \\ \frac{1}{C_1} & 0 & 0 \\ -r_{C1} & -1 & 0 \end{pmatrix}, \quad \mathbf{B}_2 = \begin{pmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ 0 & r_{C1} & 1 \end{pmatrix} \quad (20)$$

$$\mathbf{x} = \begin{pmatrix} i_{L1} \\ v_{C1} \\ x_3 \end{pmatrix}, \quad \mathbf{u} = \begin{pmatrix} v_g \\ i_{\text{ref2}} \\ V_{\text{ref1}} \end{pmatrix} \quad (21)$$

6 Stability boundaries in the parameter space

Let $D_1 = D$ for simplicity of notation. Let $\mathbf{\Phi}_1(DT) = \exp(\mathbf{A}_1 DT)$, $\mathbf{\Phi}_2((1-D)T) = \exp(\mathbf{A}_2(1-D)T)$. Let us also define the matrix $\mathbf{\Phi} = \mathbf{\Phi}_2(DT)\mathbf{\Phi}_1((1-D)T)$ and the vector $\mathbf{\Psi} = \mathbf{\Phi}_2(t)\int_0^{D_1T}\mathbf{\Phi}_1(t)\mathbf{B}_1\mathrm{d}t + \int_{D_1T}^{T}\mathbf{\Phi}_2(t)\mathbf{B}_2\mathrm{d}t$. In [7] has been shown that at the onset of subharmonic oscillation boundary, the following condition is fulfilled

$$\mathbf{F}_1[\dot{\mathbf{x}}(DT^-) - \mathbf{\Phi}_1(\mathbf{I}+\mathbf{\Phi})^{-1}]\mathbf{\Phi}_2\Delta\dot{\mathbf{x}}(DT) = m_{a1} \quad (22)$$

where $\Delta\dot{\mathbf{x}}(DT) = \dot{\mathbf{x}}(DT^+) - \dot{\mathbf{x}}(DT^-) = (\mathbf{A}_1 - \mathbf{A}_2)\mathbf{x}(DT) + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{u}$ whenever a solution $\mathbf{x}(DT)$, corresponding to a

periodic orbit $\mathbf{x}(t)$ at time instant DT, exists. For the boost converter $\mathbf{B}_1 = \mathbf{B}_2$. Let $\mathbf{A} = \mathbf{A}_1 - \mathbf{A}_2$. Therefore $\Delta\dot{\mathbf{x}}(DT) = \mathbf{A}\mathbf{x}(DT)$ and (22) becomes

$$\mathbf{F}_1[\mathbf{A}_1\mathbf{x}(DT)+\mathbf{B}_1\mathbf{u}-\mathbf{\Phi}_1(\mathbf{I}+\mathbf{\Phi})^{-1}]\mathbf{\Phi}_2\mathbf{A}\mathbf{x}(DT) = m_{a1} \quad (23)$$

Although the previous equation is a closed-form expression for the stability boundary, its use for design-oriented analysis is not easy. To overcome this problem, the following section provide design-oriented expression suitable for the choosing parameter values that guarantee stability in the parameter space.

7 Design-oriented stability conditions and slope interactions

In steady-state, the slope of the intermediate capacitor voltage is governed by the following equations

$$m_{C1} = -\frac{i_{\text{ref2}}}{C_1} < 0 \quad (24)$$

$$m_{C2} = \frac{i_{L1}}{C_1} - \frac{i_{\text{ref2}}}{C_1} > 0 \quad (25)$$

The slope of the output voltage of the first stage is given by

$$m_{o1} \approx -\frac{i_{\text{ref2}}}{C_1} - r_{C1}\frac{\mathrm{d}i_{\text{ref2}}}{\mathrm{d}t} \quad (26)$$

$$m_{o2} = \frac{i_{L1}}{C_1} - \frac{i_{\text{ref2}}}{C_1} + r_{C1}m_2 \quad (27)$$

From (28), the inductor current reference i_{ref1} in the first stage is given by

$$i_{\text{ref1}} = W_v(V_{\text{ref1}} - v_{o1} + \omega_{zv}\int(V_{\text{ref1}} - v_{o1})\mathrm{d}t) \quad (28)$$

whose slope during the conducting time is given by

$$m_{\text{ref1}} = W_v(-m_{o1} + \omega_{zv}(V_{\text{ref1}} - v_{o1})) \approx -W_v m_{o1} \quad (29)$$

where in the last expression it has been considered that $v_{o1} \approx V_{\text{ref1}}$ and that i_{ref2} is constant. Therefore the new expression for the minimum ramp needed to avoid subharmonic oscillations in a current mode controlled dual-stage cascaded boost converter is given by the following expression

$$\underbrace{\frac{v_{o1}(D)}{L_1}(D-\frac{1}{2}) - W_v\frac{i_{\text{ref2}}}{C_1}}_{m_{a,\text{cri,new}}(D)} < m_a \quad (30)$$

Figure 8 shows the boundary between stable and unstable regions in the parameter space (D, m_{a1}) for different values of W_v and C_1 obtained from (23). The new critical value is smaller than the traditionally used. Therefore a classical design procedure can predict subharmonic oscillation while the system is still stable. The new design-oriented expression (30) is more accurate.

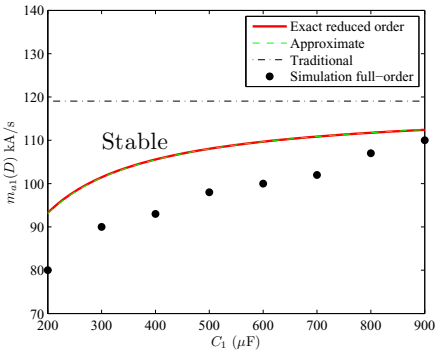


Fig. 8. Boundary between stable and unstable regions in the parameter space (C_1, m_{a1}).

8 Conclusions

High conversion ratio cascaded boost converters are applied in a broad range of applications. The advantage of using cascaded converters is that a desired output voltage/current can be obtained with higher efficiency than in single stage systems and that a specified variation in output voltage can be realized faster and more precisely. The penalty is the added complexity that follows from using a large number of components and the interaction between the different stages. In this paper an investigation of the dynamics of a cascade connection of current mode controlled boost converters is performed. A reduced-order model has been obtained allowing the obtaining closed-form expressions for the stability boundaries.

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