

# Fracture mechanics in new designed power module under thermo-mechanical loads

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**Abstract.** Thermo-mechanically induced failure is a major reliability issue in the microelectronic industry. On this account, a new type of Assembly Interconnected Technology used to connect MOSFETs in power modules has been developed. The reliability is increased by using a copper clip soldered on the top side of the chip, avoiding the use of aluminium wire bonds, often responsible for the failure of the device. Thus the new designed MOSFET package does not follow the same failure mechanisms as standard modules. Thermal and power cycling tests were performed on these new packages and resulting failures were analyzed. Thermo-mechanical simulations including cracks in the aluminium metallization and intermetallics (IMC) were performed using Finite Element Analysis in order to better understand crack propagation and module behaviour.

## 1. Design of the power module

The power module used in this study is a newly designed MOSFET package. It has an electric connection achieved by a copper clip soldered on top of the chip instead of using a wire bond.

## 2. Experimental tests

Thermal cycle testing refers to situations where the environmental surrounding of the power module undergoes cyclic thermal variations. Here, accelerated passive thermal cycles were performed. These consist of a dwell at a high temperature, a ramp to a low temperature, a dwell at the low temperature, a ramp to the high temperature, and then the cycle is repeated. In contrast, power cycling refers to situations where the heat source is the electronic package itself. The package has a chip that is powered and thus dissipates heat through the entire module. Both temperature and power cycling were performed on modules and the following failures were observed: cracks in chip, delamination between mold and Cu-leadframe, solder degradation, cracks in mold, delamination and degradation of chip metallization and intermetallic (IMC). Some of these failures are well known in microelectronics [1, 2]: cracks in chip

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Figure 1. a) Inner structure and b) layer composition of a MOSFET with a copper clip.

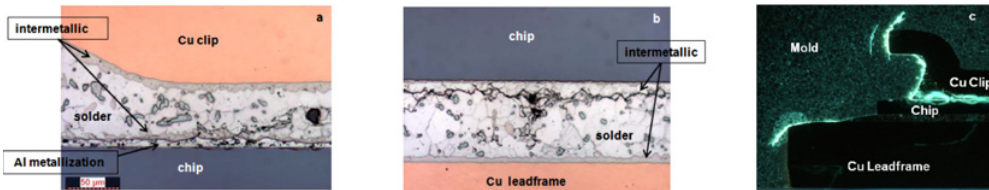


Figure 2. a) Crack in chip metallization, 2b) crack in bottom solder, 2c) delamination mold-Cu leadframe, mold-solder meniscus, crack in chip metallization and cracks in mold (dye penetrant inspection with UV microscope).

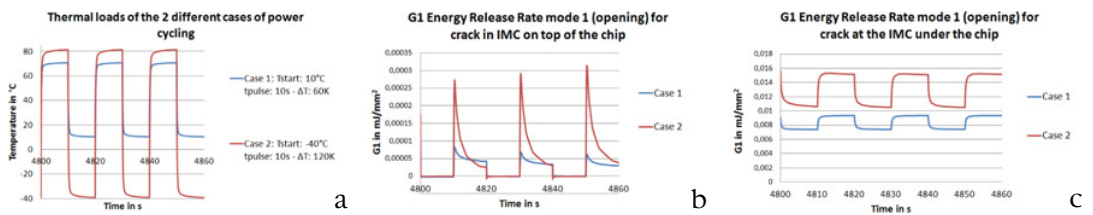


Figure 3. Thermal loads of the 2 cases of power cycling, 3b) energy release rate at the crack in IMC on top of the chip, 3c) energy release rate in the crack at the IMC under the chip.

induced by sawing, and delamination between mold and Cu-leadframe. Solder degradation is a critical failure induced by temperature cycling. Cracks in mold hardly ever happen, but can cause other failures in the device, like solder delamination. Degradation and delaminations in chip metallization and IMC are due to power cycling.

### 3. Numerical simulations

In order to simulate power cycling, a 2D Finite Element Model of a MOSFET has been created with an axisymmetric condition. Cracks were included in the IMC layer on top of the chip and at the interface between the chip and the IMC below. For those cracks the Virtual Crack Closure Technique (VCCT) is used to determine the energy release rate [3]. Later, another crack will be defined in the chip metallization, and the Crack Tip Opening Displacement (CTOD) method will be used [4]. Two different cases of power cycling were simulated in order to determine the influence of test parameters (start temperature  $T_{start}$ , temperature swing  $\Delta T$  and pulse width  $t_{pulse}$ ) on failure mechanisms. For both cracks in the IMC, the power cycling case with a bigger temperature swing reaches a higher value of energy release rate. So high temperature swings are more critical for the module. Then, by comparing the criterion values for each crack, one can see that the energy release rate for the opening mode is much higher for the crack at the IMC under the chip than for the crack in the IMC on top of the chip.

## 4. Conclusions

Simulations with different tests parameters were performed and it results in different stresses and fracture criterions. Based on that, life time models can be developed with correlation of EOL tests.

## References

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