MATEC Web of Conferences **97**, 01046 (2017) DOI: 10.1051/matecconf/20179701046
ETIC 2016

Low Power CMOS Operational Amplifier with Integrated Common-Mode Feedback for Data Converter

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Abstract. The development a high-performance design of analog circuits becomes increasingly challenging with the continuous trend towards reducing the voltage supply and low power consumption without neglecting the trade-off among other performance parameters. This paper presents the design and implementation of CMOS operational amplifier (op-amp) with integrated common-mode feedback (CMFB) circuit for data converter using 0.13-µm Silterra CMOS technology. The folded cascode topology is employed as a main op-amp design because it provides high gain and high bandwidth besides low power consumption. The simulation results indicate that the DC gain of 64.5 dB along 133.1 MHz unity gain bandwidth (UGB) is achieved for a 1 pF load capacitor. The slew rate of 22.6 V/µs, the phase margin (PM) of 68.4 ° with settling time of 72.4 ns are obtained. The power consumption of this op-amp is 0.3 mW through voltage supply of 1.8 V.

1 Introduction

Wireless Operational amplifier is a core element and integral part for most analog and mixed-signal systems. The behavioral of op-amp such as high gain, high input impedances, low output impedance, high bandwidth and fast settling makes this device often used amongst multiplicity of applications like in pipeline ADC. Traditionally, op-amp can be classified into several topologies which are telescopic, folded cascode, two-stage and gain-boosted [1]. Each topology has their own compensation, but they can be applied in any design op-amp circuit by considering the performance parameter.

A telescopic op-amp is a simple topology and provided a high gain as well faster performance [2, 3]. This topology is called as 'telescopic' because the cascades are attached between the voltage supplies with the transistor in the differential pair, occurs in a structure where each branch of the transistor connected directly together in a straight line [4]. Commonly the telescopic topology has a slighter swing because of lesser current legs and produces a small power consumption and low noise.

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In a folded cascode op-amp, the topology is normally customized from the telescopic op-amp and it issues higher gain and performance [5,6] compared to the telescopic because it consumes more currents legs. This topology is called 'folded cascode' because of small signal current is folded up or to down [1]. Generally, this op-amp allows the particular input common-mode level of being near to the voltage supplies as well as performing a high output swing, wide input common-mode range and preferably steering in low voltage supply circuits [4]. However, this topology contributed greater noise that effect from the more currents legs.

2 Design constraints

A design constraint is a key element in preparing the best performance of op-amp circuit. As a requirement of a high speed and high accuracy in pipeline ADC, there are numerous constraint parameters that should be considered such as gain, unity gain bandwidth, phase margin, slew rate and also output swing. Each parameter constraints are explained as follows.

2.1 Gain

Ideally, the gain is the product of the transconductance structure over the output resistances of the load structure that express as:

$$Gain = G_m \times R_{out} \tag{1}$$

where the gain extremely depends on the frequency of the input signal of an amplifier.

2.2 Unity gain bandwidth

The unity gain bandwidth state that the frequency at which the open loop gain of the amplifier is unity with the maximum capacitance at the output node. Thus the UBW is obtained as:

$$UBW = 2\pi f C_L \tag{2}$$

2.3 Phase margin

The purpose of phase margin (PM) is to determine the stability of the amplifier where the higher values of PM will allow the output signal to achieve a stable state without much swing. Noted that the PM is depends on the applications [1].

$$Phase\ margin\ (PM) = \tan^{-1}\left[gm / (2\pi f C_L)\right] \tag{3}$$

2.4 Slew rate

Slew rate is defined as the rate of change in the output voltage that caused by a step change on the input. It can be determines by the output capacitance and the current across the output branch.

$$Slew\ rate = I_{out} / C_L \tag{4}$$

2.5 Output swing

This constraint relates to the output of the op-amp where the saturation voltage of load structure mainly defines the output swing of the op-amp. Commonly, most systems employing op amps require large voltage swings to accommodate a wide range of signal amplitude [1].

$$Output\ swing = (V_{DD} - V_{max/min}) / 2 \tag{5}$$

3 Design implementation

According to the op-amp specifications as presented in Table 1, the desired op-amp topology was determined. Folded cascode topology idyllically to be principle op-amp for this work since the design has been used in [7] for obtaining fast settling, high gain and high unity gain bandwidth besides low power consumption.

Table 1. Op-amp Specifications for Pipeline ADC.

Parameter	Value
Voltage supply	1.8 V
V_{in}	1.2 V
V_{out}	1.2 V
DC gain	> 70 dB
Phase margin	> 60º
Unity gain bandwidth	> 130 MHz

The architecture of folded cascode op-amp with common-mode feedback is illustrated as Fig. 1. Traditionally, the folded cascode op-amp has been designed by using a pair of PMOS type or NMOS type for the input range of op-amp through the limits of input common mode range [7]. For this work, the NMOS type is chosen to be an input of the differential amplifier since this input type can assign more large output gain compare to PMOS input type.

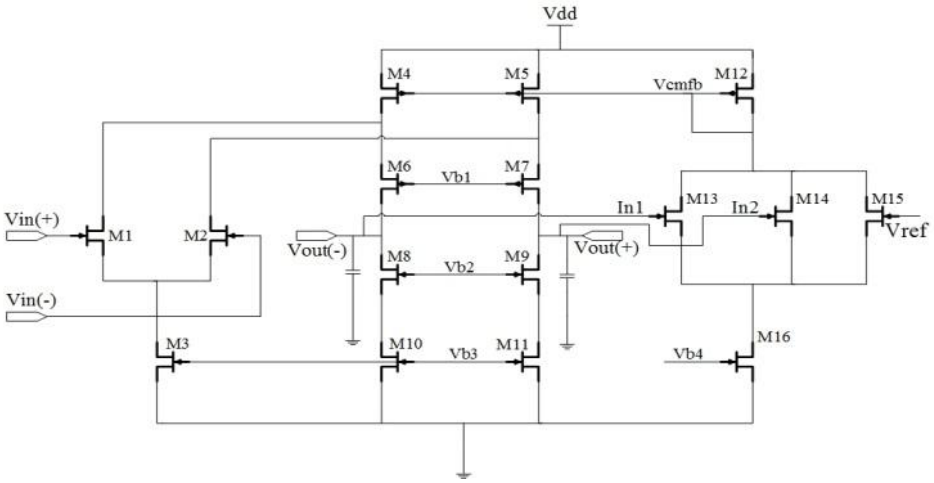

Fig. 1. Folded cascode op-amp with CMFB architecture.

As shown in Fig. 1, the folded cascode topology consists of two different structures which are NMOS differential amplifier (M1-M3) and folded cascode structure (M4-M11). The open loop voltage gain can be determined as:

$$A_v = g_m \times R_o \tag{6}$$

where g_m is a short-circuit transconductances of the output current gain across the transistor of M6 and R_o is the output impedance of folded cascode by looking into the drains of M6 and M8.

$$R_o = g_{m6}.r_{o6}(r_{o1}||r_{o4}) \;||\; (g_{m8}.r_{o8}.r_{o10}) \tag{7}$$

Therefore, the gain is expressed as:

$$A_v = g_m\{[g_{m6}.r_{o6}.(r_{o1}||r_{o4})] \;||\; [g_{m8}.r_{o8}.r_{o10}] \tag{8}$$

Meanwhile, the gain bandwidth of the folded cascode circuit is:

$$GBW = g_{m1} / C_L \tag{9}$$

where g_{m1} is a transconductance of M1 and C_L is the capacitance at the output node.

A CMFB circuit (M12-M16) is designed in order to fix the voltages at high impedances node to the desired voltage value of CMRR performance while ensuring the stability of common-mode voltage for fully differential op-amp [8]. As referred in Fig. 2, M12 is assigned to be a feedback to the folded cascode op-amp while M13 and M14 is an input of CMFB that attaches to the output of folded cascode op-amp and M15 represents as a reference voltage. This CMFB architecture is modified from the conventional amplifier as

in Fig. 1(a) in [9]. The modification is based on M12 because its need a stable voltage to fed the folded cascode op-amp. Subsequently, these two circuit blocks are implemented in 1.5-bit per stage pipeline ADC as shown in Fig. 2 in order to simulate the circuit performances. The result is discussed in section below.

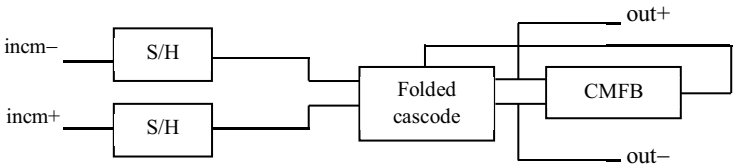

Fig. 2. Implementation circuit in 1.5-bit per stage pipeline ADC.

4 Results and discussion

The proposed folded cascode op-amp was designed using Cadence Software and implemented in 0.13-µm process technology with 1.8 V supply voltage whereas the simulation of circuit via Cadence Virtuoso spectre. The circuit design is analyzed in two methods which are AC analysis and Transient analysis. Fig. 3 shows the AC analysis result of the proposed circuit. The simulated DC gain demonstrated 64.5 dB with 68.4 degrees of phase margin (PM) as shown in Fig. 3 (a) and Fig. 3 (b), respectively. Meanwhile, the transient analysis result is depicted in Fig. 4. The slew rate performs 22.6 V/µs among 72.4 ns of settling times.

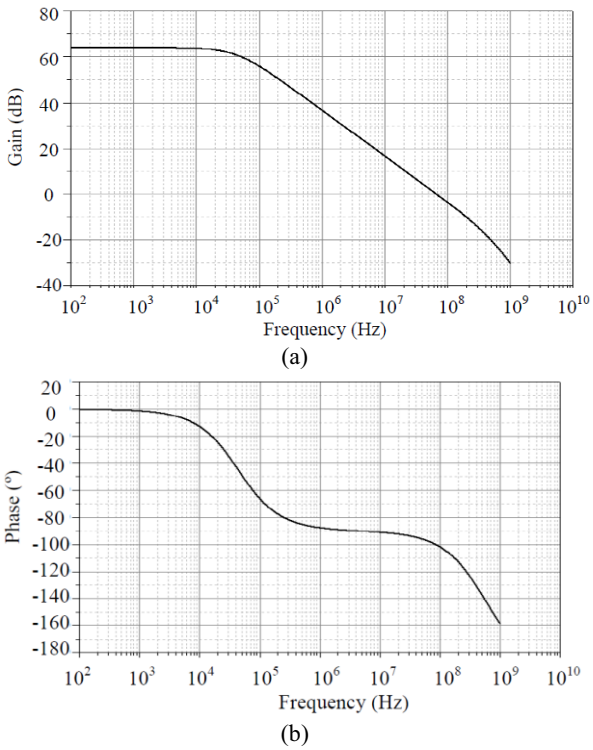

Fig. 3. AC analysis: (a) Gain, (b) Phase margin.

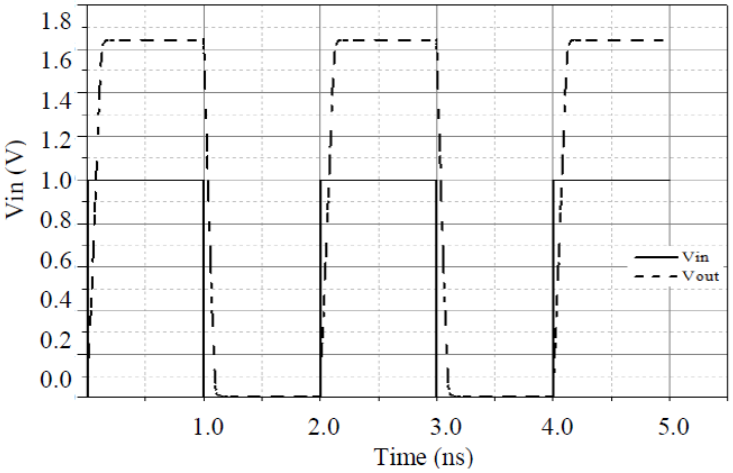

Fig. 4. Transient analysis.

Table 1 Fig. 5 illustrates the result for implementation of the circuit in 1.5 bit per-stage pipeline ADC. The performances of the circuit are referring to the process information as tabulated in Table 2.

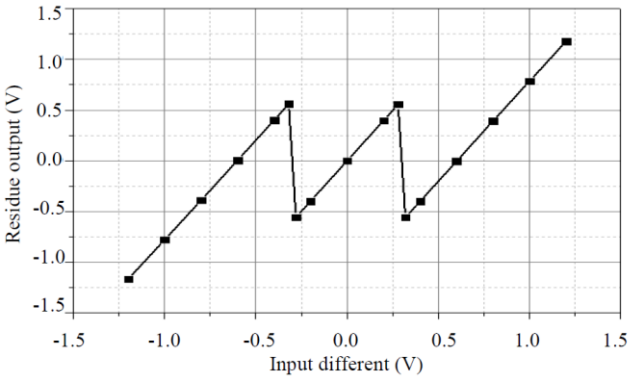

Fig. 5. Implementation results.

Table 2. Data converter information for 1.5-bit per stage pipeline ADC.

Vin	B1	B0	DAC output	Residue output
Vin > Vref/4	1	0	+Vref	0.18
-Vref/4 < Vin < Vref/4	0	1	0	1.0
Vin < -Vref/4	0	0	-Vref	2.4
Vin > Vref/4	1	0	+Vref	9.0

The comparison for folded cascode op-amp performances between previous works is summarized as in Table 3. From the table, this circuit design attains low power consumption with smallest load capacitance; therefore the chip size can be reduced.

5 Conclusion

The design and implementation of CMOS op-amp with integrated common-mode feedback circuit for data converter using 0.13-µm Silterra technology is presented. The DC gain of the op-amp is obtained about 64.5 dB along with unity gain bandwidth (UGB) of 133.1 MHz for a 1 pF load and 68.4 degrees. The circuit in this work consumes a low power consumption which is around 0.3 mW at 1.8 V supply supply. The simulation result shows that the proposed design is suitable for data converter applications.

Table 3. Folded cascode op-amp performances.

Reference	**[10]**	**[11]**	**[12]**	**[6]**	**This wok**
Technology (µm)	0.18	0.18	0.13	0.13	0.13
V_{DD} (V)	1.8	1.8	3.0	1.8	1.8
DC gain (dB)	90.30	50.97	94.9	91.5	64.5
Unity gain Bandwidth (MHz)	700.7	944.0	41	714.5	133.1
Phase margin (º)	63.85	75.9	82.3	62.0	68.4
Slew rate (V/µs)	N/A	712.5	N/A	N/A	22.6
Settling time (ns)	N/A	N/A	6.17	40.0	72.4
Power consumption (mW)	3.24	172.8	11.0	9.0	0.3
Load capacitance (pF)	0.5	2.4	2.0	7.5	1.0

This work was financially supported by the Fundamental Research Grant Scheme (9003-00387).

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