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ON THE SELECTION OF OPTIMAL STRUCTURE ORGANIZATION OF LOGIC MULTICONTROLLERS

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Abstract. In the article the basic approaches to structural-parametric optimization of logical control systems in the basis of logical multicontrollers were given. Based on the results of a series of computational experiments we obtained the set of dependencies on the deterioration of the quality criteria of separations of graph-schemes of parallel logic control algorithms and corresponding parameters values of LMC from technological restrictions on the controller structure. It is shown that the structure of the LMC with a large number of simple controllers is preferred.

1 Introduction

One of the promising approaches to the synthesis of logic control systems (LCS) is their implementation in the basis of logical multicontroller (LMC) [1] which are interconnected in the collective working in parallel similar controllers together solving the problem to implement epy given logic control algorithm presented by corresponding graph-scheme. When designing such multisystems there is a number of discrete combinatorial optimization problems [2–5]. One of them is the problem of getting suboptimal separation of a priori known graph-scheme of parallel logic control algorithm to sequential blocks with restricted complexity, each of which is implemented by one of the controllers within the LMC [6–9]. This problem relates to the NP complexity class that does not allow to find the optimal solution for its practical dimension cases (graph-schemes with more than 10–20 vertices) at a reasonable time, therefore its solutions are known and have been successfully used with various heuristic approaches [2–4, 10] having different implementation complexity, asymptotic time and memory complexities of corresponding algorithms, set of optimized partial quality criteria and integral quality of the obtained solutions. The quality of separations directly affects the hardware complexity of the LMC and its speed characteristics.

During LMC design can be used two different approaches. According to the first of them the structure of LMC (number of modules and its hardware characteristics, topology

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of the connections between them, redundancy options, etc.) is selected once, based on the specific graph-scheme of control algorithm and selected separation for the implementation of which it is necessary to create appropriate LCS. Numerical parameters of separation (number of blocks and links between them) determine the hardware requirements for LMC, and when you change the control algorithm selection LMC structure is actually made anew. This approach can be used, for example, as a way of implementation of control part for specialized computing device with ASIC based production the operating part of which is selected at the design stage and is not changed during further operation. According to the second approach the structure of LMC is generalized and focused on the implementation of one of the group of control algorithms by software setting that makes it possible to change the control algorithm without changing the hardware structure of LMC during operation. This approach can be used, for example, as implementation of assembly line control system in which the set of operations may vary with time. From the standpoint of producer of these LCSs named as programmed logic controllers (PLC) it is interesting to the development of the model range formed by a group of products with different cost and performance characteristics. At the same time design engineer of control part has the opportunity to select one of the LMC models within corresponding model range enough to please it as a cost and the possibility of implementing of the needed control algorithm. Easy to see that the first approach is the analogue of well known ASIC approach that is characterized by rather a high cost while the second one is essentially similar to the practical use of logical circuits with reconfigurable structure such as FPGAs (Field-Programmable Gate Array) and ULAs (Uncommited Logic Array) [11] that can significantly reduce the cost of the final solution for its practical use.

When choosing an appropriate model range a number of issues is arisen connected with structural-parametric optimization of forming its multicontrollers and selecting its structure organization corresponding to practical requirements. For example, when a physical limitation (balance requirements) by the number of transistors, metallization layers on a chip, requirements of electromagnetic and/or thermal compatibility of electronic components and so on you must choose such a structure of LMC that will be characterized by low production costs (for example, with a small area on a chip) and at the same time allows the implementation of a particular group of control algorithms (for example, with selected number of vertices, control signals and speed characteristics) without the need to change the current model of composed model range for more expensive one on the one hand and on the other performance degradation on the another hand. In its simplest form, the need to choose such a structure leads to specifying the number of controllers within the LMC and its hardware performance, while maintaining the given hardware complexity of multisystem within the prescribed limits. In other words, it is possible to implement the LMC, which includes all other things in its structure being equal a large number of relatively simple controllers, a small number of complex controllers or a compromise version. Structural-parametric optimization of LMC can be achieved by finding the number of separations of logic control algorithms, statistical processing of the results and analysis of changes in average quality criteria trends depending on technological restrictions arising in selecting the appropriate structure of LMC.

2 Statement of a problem

A formal presentation of the problem of getting separation has the following form. It is required to obtain a separation $Sep\left(A^0\right)=\left\{A_1, A_2, ..., A_H\right\}$ of the set of vertices A^0 for

source graph-scheme of parallel logic control algorithm $G^0 = \langle A^0, V^0 \rangle$ satisfying the following conditions:

$$\begin{gathered} \bigcup_{i=1}^{H} A_i = A^0, \quad A_i \neq \varnothing, \quad A_i \cap A_j = \varnothing, \quad i, j = \overline{1,H}, \quad i \neq j, \\ \neg(a_i \omega a_j) \; \forall a_i, a_j \in A_k, \quad i \neq j, \quad k = \overline{1,H}, \\ W(A_i) \leq W_{\max}, \quad |X(A_i)| \leq X_{\max}, \quad |Y(A_i)| \leq Y_{\max}, \quad i = \overline{1,H}, \end{gathered} \tag{1}$$

where ω – designation of a binary relation of vertices parallelism [1] reflecting a structural restriction of LMC on the prohibition of parallel vertices within blocks of separation, $W(A_i) = \sum_{a_j \in A_i} W(a_j)$ – summary "weight" of vertices within the *i*-th block (size in controller memory measured at microcommands); $X(A_i) = \bigcup_{a_j \in A_i} X(a_j)$ – a set of logical conditions included in the vertices within the *i*-th block; $Y(A_i) = \bigcup_{a_j \in A_i} Y(a_j)$ – a set of microoperations included in the vertices within the *i*-th block, $W_{\max}$ – constraint in the memory capacity of the controller as part of LCS, $X_{\max}$ – constraint in the number of signals of logic conditions received by the controller, $Y_{\max}$ – constraint in the number of microoperation signals issued by the controller, such that

$$\begin{gathered} Z_H = H(Sep(A^0)) \to \min, \\ Z_\alpha = \sum_{i=1}^{H} \sum_{j=1, j \neq i}^{H} \alpha(A_i, A_j) \to \min, \\ Z_\delta = \delta(Sep(A^0)) \to \min, \\ Z_X = \sum_{i=1}^{H} |X(A_i)| - |X(A^0)| \to \min, \\ Z_Y = \sum_{i=1}^{H} |Y(A_i)| - |Y(A^0)| \to \min, \end{gathered} \tag{2}$$

where $Z_H = H(Sep(A^0))$ – the number of blocks in the separation; Z_α – complexity of the interconnect network for separation $Sep(A^0)$; $\alpha(A_i, A_j)$ – coupling coefficient of blocks pair (it is equal to 1 if the blocks are connected by the control in direction from A_i to A_j, which requires an additional command for transfer of control between controllers, and 0 otherwise); $Z_\delta = \delta(Sep(A^0))$ – the total number of interblock interactions (summary interblock traffic); Z_X – the extent of duplication of logical conditions signals; Z_Y – the extent of duplication of microoperations signals. Minimizing these partial quality criteria can decrease hardware complexity of LCS (criteria Z_H, Z_X, Z_Y, Z_α) by reducing the required number of controllers, complexity of interconnect network and hardware complexity of separate controllers, and improve performance of LCS (criterion Z_δ) by reducing control traffic and communication subsystem loading.

Number of blocks within the separation provides the number of microprograms and accordingly, the number of controllers within LMC, each of them implements one of them. In the absence of technological restrictions $(X_{\max} = Y_{\max} = W_{\max} = \infty)$ a number of blocks

in separation has low theoretically limit that is provided by the value of the parallelism degree of graph-scheme of parallel algorithm $\omega_{\max}\left(A^0\right)$ [1].

3 Computation experiments overview

For each of the heuristic methods [1–4, 10] set of test examples (graph-schemes of parallel control algorithms) can be selected in which they demonstrate the highest quality of solutions compared with other methods, so the specified type of comparison methods is sufficiently subjective. Therefore, in order to realize the objective of comparing the quality of separations given by different heuristic methods with different using conditions we will carry out a comparison of average values of quality criteria of separations using a generator of graph-schemes of algorithms with selected parameters (number of vertices, microoperations and logic conditions signals, probabilities of fragments with different type, etc.) and pseudorandom structure working within program system PAE. Using this generator it is possible to obtain samples $\Lambda = \left\{G_1^0, G_2^0, ..., G_K^0\right\}$ of graph-schemes of an arbitrary amount K of control algorithms that in its turn provides the ability of objective comparison quality of separations given by different heuristic methods and track the trends in the partial values of quality criteria when changing the values of technological restrictions $X_{\max}$, $Y_{\max}$ and $W_{\max}$ and size of a problem N. For the selected conditions of the computational experiment and this method of getting separations it is possible to determine the partial sample average quality criteria values γ_x and probabilities of getting minimum value of selected partial quality criterion ρ_x, $x \in \{H, X, Y, \alpha, \delta, J\}$, where J – designation of integral quality criterion of separation $Sep\left(A_k^0\right)$ [1]

$$J\left(Sep\left(A_k^0\right)\right) = \frac{K_H}{\omega_{\max}\left(A_k^0\right)}H + \frac{K_X}{\left|X\left(A_k^0\right)\right|}\left(\sum_{i=1}^{H}\left|X\left(A_i\right)\right| - \left|X\left(A_k^0\right)\right|\right) + \\ + \frac{K_Y}{\left|Y\left(A_k^0\right)\right|}\left(\sum_{i=1}^{H}\left|Y\left(A_i\right)\right| - \left|Y\left(A_k^0\right)\right|\right) + \frac{K_\delta}{\delta\left(A_k^0\right)}\delta\left(Sep\left(A_k^0\right)\right) + \\ + \frac{K_\alpha}{\omega_{\max}\left(A_k^0\right)\left(\omega_{\max}\left(A_k^0\right)-1\right)}\sum_{i=1}^{H}\sum_{j=1,\ i\neq j}^{H}\alpha\left(A_i, A_j\right), \tag{3}$$

which is a weighted sum of normalized partial quality criteria. Here $K_H, K_X, K_Y, K_\alpha, K_\delta$ – weighting coefficients that are selected by experts and reflecting the importance of partial quality criteria; $\delta\left(A_k^0\right)$ – the theoretical maximum intensity of interblock interactions achieved in the separation where each vertex of control algorithm forms a separate block.

In a series of computational experiments that are computationally complex (the amount of computation is required hundreds of years of CPU time) and is performed using a grid system on a voluntary basis within volunteer distributed computing project Gerasim@home at BOINC platform [12] it was shown that quality of separations and probabilities of getting best decisions vary significantly for different heuristic methods and for different regions of space (Figure 1) formed by the size of the problem N and values of technological restrictions $X_{\max}$ and $W_{\max}$ (restriction $Y_{\max}$ can be simply avoided by doubling the controller within LMC [1]).

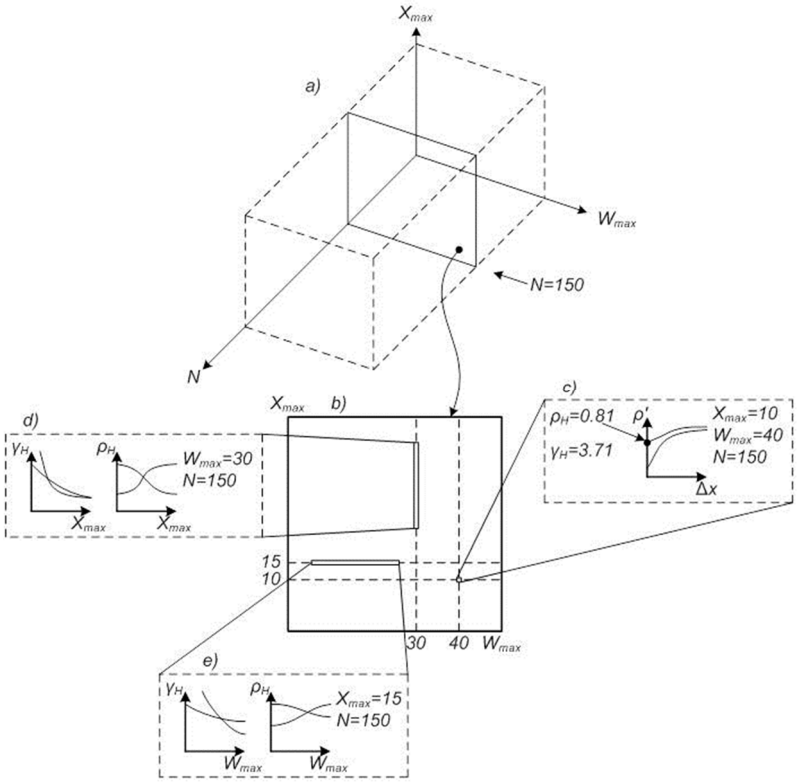

Figure 1. Space of parameters (a), map of the slice $(X_{\max}, W_{\max})$ (b) and early one parameter computational experiments (c, d, e).

4 Analysis of computation experiments results

General view of the dependency of partial quality criterion from the dimension of the problem and the value (power) of technological restriction is shown in Figure 2.

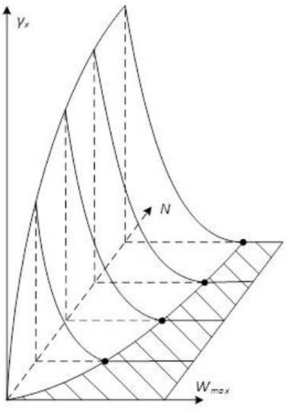

Figure 2. The general behavior of partial quality criteria *Z* depending on size of the problem *N* and power of constraint ($W_{\max}$ in this example). Shaded area shows the area of insensitivity.

At low values of technological restrictions $\left(X_{\max}, W_{\max} \to \infty\right)$ quality of separation is independent from the technological restrictions and other factors (such as structure restrictions of LMC basis and parameters of source graph-scheme G^0). During increasing power of restriction $\left(X_{\max}, W_{\max} \to 0\right)$ values of partial quality criteria begin to increase monotonically. In the area of insensitivity (shown at Figure 2 shaded) changes of partial quality criteria does not occur that allows to optimize structure of LMC by formulating requirements for limiting values $X'_{\max}$ and $W'_{\max}$ of technological restrictions for selected size of graph-schemes of logic control *N*. So when $\left(X_{\max} > X'_{\max}\right) \wedge \left(W_{\max} > W'_{\max}\right)$ it is an increase in hardware complexity of controllers and LCS without getting the smaller values of partial quality criteria of partitions that is inappropriate.

In the article [13] as a result of computing experiments boundaries of insensitivity area were obtained. They are based on results of separations, obtained using the method of parallel-sequential decomposition as having minimal values of $X'_{\max}$ and $W'_{\max}$ from all other methods, and allows to formulate the hardware requirements for controllers within LMC with matrix structure (as an example). For example, controllers within matrix LMC with $7 \times 7 = 49$ modules must have 120 memory cells (command words) for microprogram storing (that corresponds to source graph-scheme of control algorithm separated by blocks) and 86 pins for receiving logic condition signals from controlling object that allows to implement graph-scheme with 450 vertices.

Decreasing values $X_{\max}$ and $W_{\max}$ less than the limits (for example, because of the inability or inexpediency production of LMC in the hardware configuration of the technological or cost reasons) leads to growth of partial quality criteria values (see Figure 2) that reduces the speed of the designed LCS due to the increasing control transfer traffic between controllers, increases hardware complexity of communication subsystem of controllers due to the need to implement a greater number of inter-module commands of the control transfer and greater depths of corresponding queues, and also requires the implementation of a larger number of controllers in comparison with a theoretical lower limit $\omega_{\max}\left(A^0\right)$. This is quite an important study showing how this or that partial quality criteria value deteriorates during increasing power of restrictions (decreasing values $X_{\max}$ and $W_{\max}$). The answer to this question is obtained while processing the results of a series of computation experiments and shown at Figures 3 and 4, where level lines marked as $F_{z\%}$ correspond to decreasing quality of decision by $z\%$ comparing to theoretical minimum that provided by method *F* for selected size of a problem *N*. These dependences allow a quantitative study of the characteristics of separations during decreasing values of technological restrictions.

An analysis of given results allows to conclude that decreasing quality of decisions for parallel-sequential method in relative units is lower than the same results by S.I. Baranov method and greedy adjacent method. Methods that are based on greedy strategy of building separation shows significantly more deterioration in the quality of decisions on criteria of interblock links number and intensity of interconnect control traffic, especially during reducing the limit value of the controller memory capacity $W_{\max}$. As we have noted previously [13], values $X'_{\max}$ and $W'_{\max}$ for parallel-sequential method [1] are closer to zero (respectively, its insensitivity zone is wider) comparing to variations of greedy approaches.

This feature allows to recommend the method of series-parallel decomposition to practical use as providing a minimal increase of quality criteria values during decreasing values of technological restrictions [14].

In practice, it is more important not simply start making deterioration but deterioration in the presence of any predetermined value, empirically selected by the developer of LCS. For example, during performing program optimization of software empirical limit of decreasing time complexity is value of 5% [15] and optimizations providing less decrease are often ignored due to the fact that they are characterized by unpredictable behavior of the speed characteristics of the programs within the time interval measurement error. Assuming deterioration of the integral criterion J within 5% from theoretical limit the technological restrictions can be significantly reduced in comparison with [13], as shown in the Table 1.

For example, above mentioned configuration of LMC with 7×7 controllers limits to a number of received logical condition signals decreased from 86 to 5 pins and limits to volume of memory – from 120 to 21 command words that allows significantly (some times less) decrease the hardware complexity of controllers within LMC and total hardware complexity of LCS at the cost of 5% deterioration in the quality of partial quality criteria (for example, speed characteristics of hardware complexity of communication subsystem).

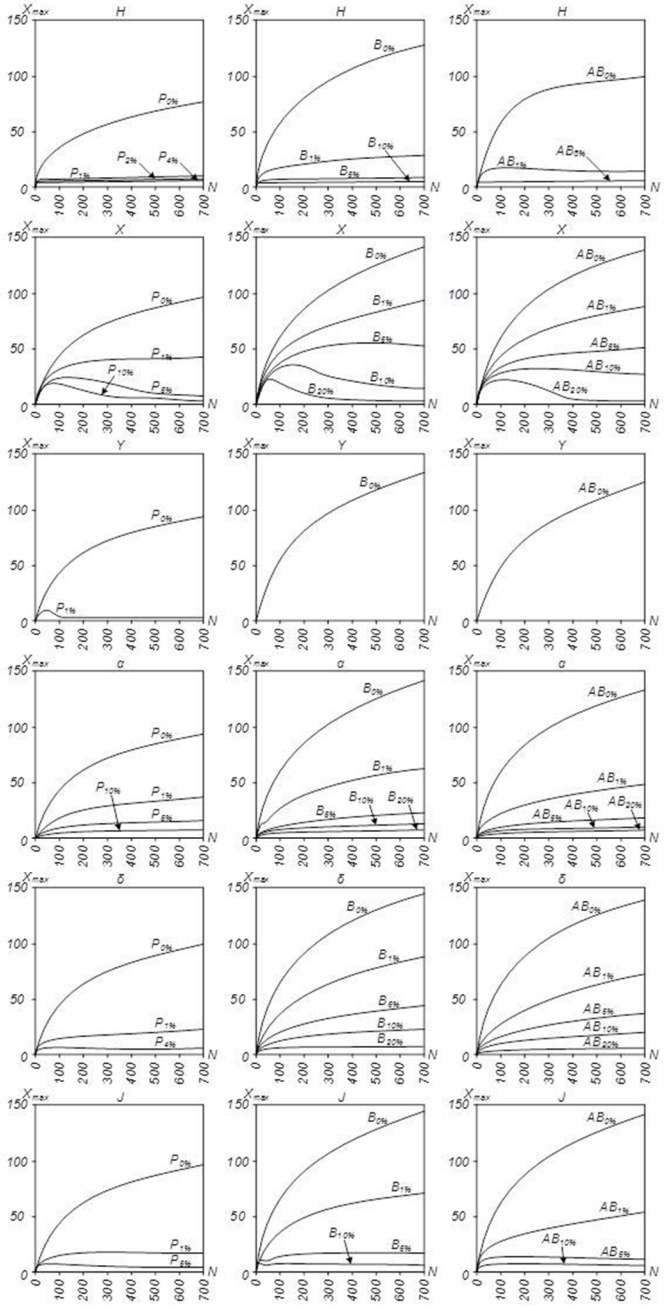

Figure 3. Increasing values of quality criteria during decreasing value $X_{\max}$ in percents from quality of corresponding criteria with $X_{\max} = \infty$. Here P – parallel-sequential method [1], B – S.I. Baranov method [10], AB – greedy approach with adjacent neighborhood.

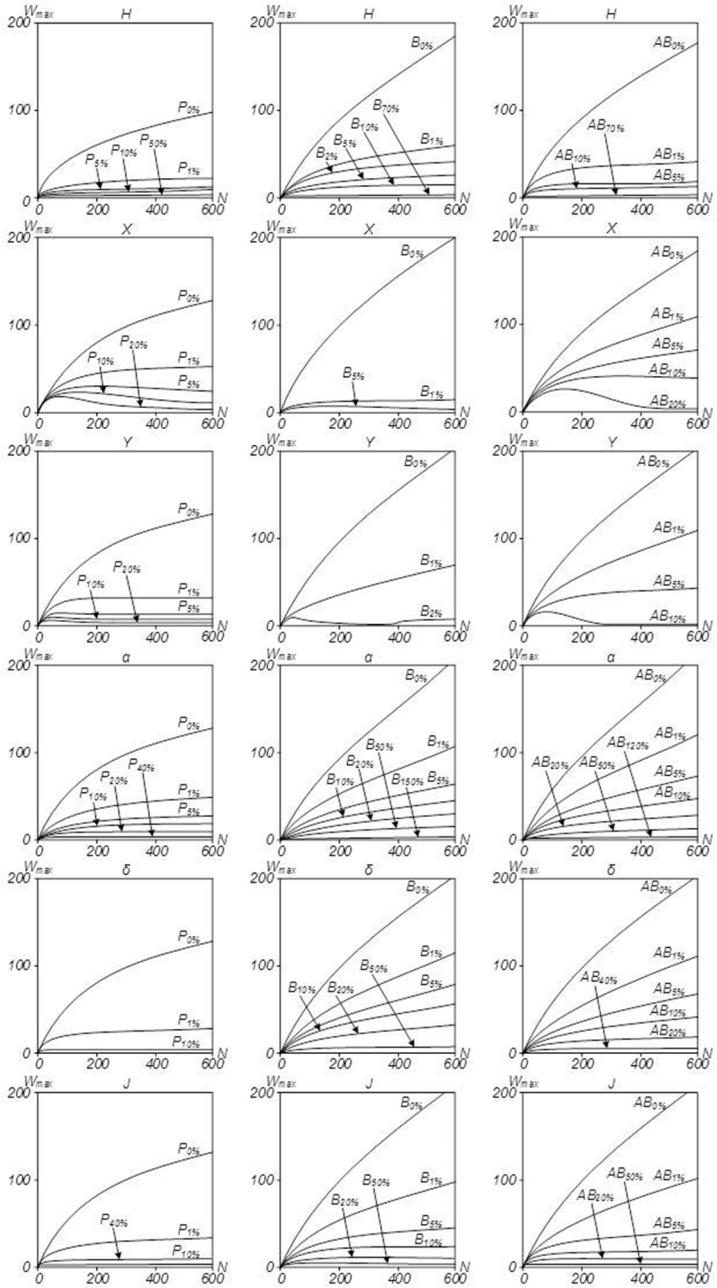

Figure 4. Increasing values of quality criteria during decreasing value $W_{\max}$ in percents from quality of corresponding criteria with $W_{\max} = \infty$.

Table 1. Comparison of given limits for zero cases [13] and 5% deterioration of the integral quality criterion.

Number of controllers (H) within multicontroller without redundancy	Average number of vertices (N) within graph-scheme, no more than (where $X_{\max} \geq X'_{\max}$ and $W_{\max} \geq W'_{\max}$)	Limit restrictions (without decreasing of integral criterion J)		Limit restrictions (allowed 5%-e decreasing of integral criterion J)	
		$X'_{\max}$	$W'_{\max}$	$X'_{\max}$	$W'_{\max}$
$3\times3=9$	50	30	34	7	13
$4\times4=16$	110	49	61	7	16
$5\times5=25$	200	64	84	6	18
$6\times6=36$	312	76	105	5	20
$7\times7=49$	450	86	120	5	21
$7\times8=56$	535	89	126	5	21

5 Conclusion

So as one of results of analysis of computational experiments data, we can conclude that for the implementation of graph-schemes of logic control with a different number of vertices it is preferably using large number of relatively simple controllers within LMC with a small number of pins for receiving logic control signals $X'_{\max}$ and small volume of microprogram memory $W'_{\max}$ that leads to no more than 5% deterioration of the quality of integral quality criterion and, accordingly, technical characteristics of LCS. Increasing complexity of the controller structure leads to the increase in hardware complexity and cost of production for LMCs and does not lead to a significant increase in performance or reduce the number of modules in the LCS and may be considered inappropriate. The number of relatively simple controllers within LMC is relatively large and very similar situation with the presence of a large number of control exchanges between controllers Z_{δ} that imposes corresponding requirements on the communications subsystem and makes important subtask of minimizing the intermodule control transfer traffic [1]. The shown experimental data (Table 1) can serve as a starting point for selecting the preferred LMC structure in the formation of the corresponding model range starting from the specific limits of technological limitations. These restrictions limit values objectively force to work in the field of strong restrictions (close to zero values), where getting the best possible solutions provides a method of parallel-sequential decomposition [1] that confirms the expediency of its use in practice in both for design the LCS within LMC basis and during performing of their structural-parametric optimization.

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