

## Study of impact of LATID on HCI reliability for LDMOS devices

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**Abstract.** This paper demonstrates electrical degradation due to Hot Carrier Injection (HCI) stress for nLDMOS devices with different Large Angle Tilted Implantation Doping (LATID) techniques for p-body. It seems that optimization of the device with LATID angle for p-body in nLDMOS is important to achieve improved HCI performance and observed that HCI degradation is minimum for 30° LATID for p-body. We observed Si/SiO<sub>2</sub> interface trap under various stress conditions, were evaluation based on our Sentaurus simulation, and we compare trapped charge density and distribution for various LATID angles and it was less for 30° tilt. Trap-related models were employed to perform Ron and Id,sat degradations during the HCI stress test. So nLDMOS device with 30° tilt angle for p-body shows better HCI performance compared to other LATID. Also our new proposed device structure shows less HCI degradations when compared with silicon data of HCI degradations for other nLDMOS structure.

### 1 Introduction

Lateral DMOS transistors are widely used as integrated high-voltage switches and drivers in mixed-signal integrated circuits. The extended drain structure with isolation either by STI or Thermo-oxide and “RESURF” technology [1] are widely used to obtain high-voltage capability while keeping low on resistance so to optimize the specific resistance versus breakdown voltage trade-off. In past, a rugged LDMOS for a 0.35µm Linear BiCMOS technology, which achieves a strongly enhanced electrical SOA, has been presented [2-3]. A buried body implant was added to suppress the parasitic bipolar transistor; hence no snapback was observed in the I-V characteristics: this important feature enables an extension of the current curves to higher drain voltages, when impact ionization at the drain side of the drift region becomes dominant. Thus, an unusual current “enhancement” is reported at large gate voltages with a subsequent saturation of the current at high drain biases. High operational drain and gate biases make the LDMOS device vulnerable to the damage caused by hot-carrier injection (HCI), and the reliability characterization in STI based LDMOS devices have recently drawn much attention [2-6]. However, very little is known on the hot-carrier injection effects in the rugged LDMOS device when it is operated in the high impact-ionization regime. Mechanism of this reliability issue was not well understood.

High kinetic energy of carriers is gained under the influence of high lateral fields in MOSFET channel and pinch-off region of the transistor. Hot carrier will be generated when non-equilibrium energy distribution is reached and impact ionization will be triggered.

Sufficient energy, approximately 3.6eV for electrons and 5.0eV for holes in silicon can be acquired by hot carriers to surmount the energy barrier at Si/SiO<sub>2</sub> interface or tunnel into the oxide and the effect will be raised when injected carriers interact with the oxide. This instability may appears and cause a device parameter shift in a long term operation of the device [3-5].

In this paper, the HCI-induced degradation of the double diffused LDMOS has been investigated for different tilt angle implantations i.e., Large Angle Tilted Implantation Doping (LATID). Special attention has been given to the impact of the current “enhancement” on the “ΔId,sat and “ΔRon and their dependence on the LATID and self-heating due to the power dissipation.

### 2 Experimental setup

The experimental setup was designed as flowchart in Fig. 2. Practically, the comparisons of the device degradation are performed by confrontation of IV curve before and after stress time on the device structures. Thus, degradation trend for on state resistance (RON) and drain current saturation (Id,sat) were calculated for different stress time (0s, 100s, 1000 s, 10,000 s and 100,000 s) but for 100s we didn’t get any shift in HCI or may be very less shift and thus we not presented HCI results for this case but we analysed remaining stress times. On-state resistances (RON) were calculated at drain and gate voltage equals to 0.1V and 5V respectively while drain current saturation calculated at 40V of drain and 5V of gate voltage.

Degradation, thermionic HCI and classical lucky electron models were invoked in the device simulation to perform

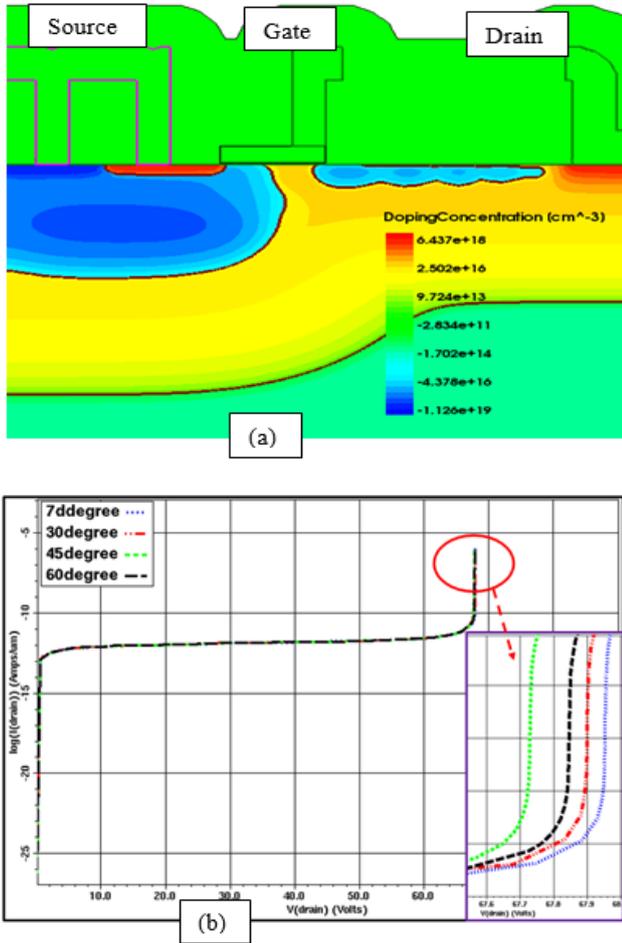
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the interface trap generation due to HCI. A process of electrons tunnel through a barrier in the presence of a high electric field was taken into account by using Fowler-Nordheim model. While, the lucky-electron model provides an estimate of the probability that some carriers in silicon will be transmitted to the oxide by overcoming the local energy barrier at the Si-SiO<sub>2</sub> interface [7-9].

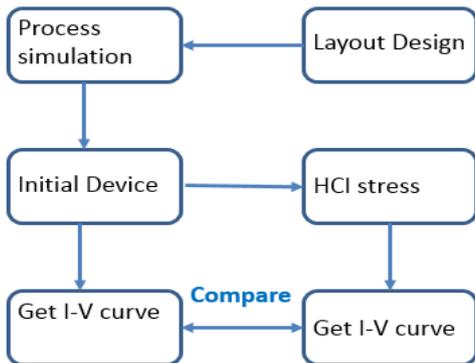
We also compared HCI results of our proposed nLDMOS structure with silicon HCI results for other nLDMOS device and we achieved better HCI results as compared to Silicon HCI results. This comparison with silicon HCI data we provide in next section of Results and discussion.

### 3 Results and discussion

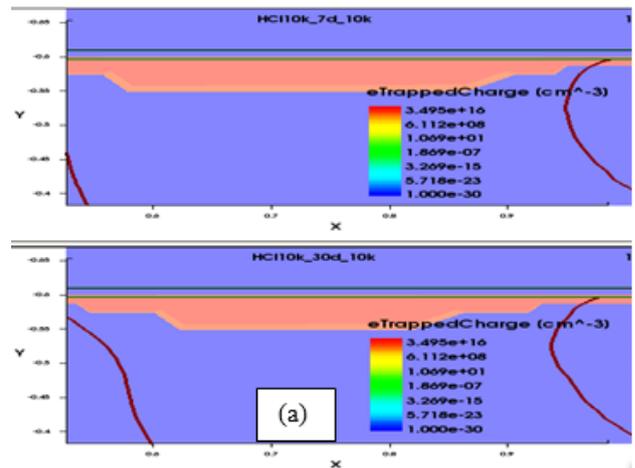
As we shown in Figure 3, Trapped charges at Si/SiO<sub>2</sub> interface are different for different LATID angle implantations. From Table 1. and Figure 3, It is clearly shows that trapped charge is least for 30° tilt and worst for 60° tilt implant. Further trapped charges for 7° and 30° seems to be equal in numerical value from Table 1 but area of trapped charges for 7° tilt is more than compared to 30° tilt. So as we know HCI degradations is because of trapped charges into the oxide region of Si/SiO<sub>2</sub> interface and HCI degradation will be more with more traps that occurs in oxide regions. Hence we got good HCI performance for 30° tilt and least for 60° tilt implant technique. We performed HCI stress test for time 0s, 1e3s, 1e4s and 1e5s and measured on-resistance shift/degrade ( $\Delta R_{on}$ ) and drain saturation current shift ( $\Delta I_{d,sat}$ ) and we summarize all HCI results with different LATID angles in Table 1. When we analyse the results we can explain that our new nLDMOS structure shows very good HCI performance. For instance Ron shift for 1e5 seconds HCI stress is 0.057%, which is best and  $I_{d,sat}$  shift for HCI 1e5 seconds is 0.398% both for 30° tilt angle. So these results very good for HCI stress test concern. It is possible for us to achieve this HCI performance because we put lot of effort to redesign the device so that impact-ionization hotspot should happen at location away from gate and below the surface so that the hot carriers that generate and experience high lateral applied field should not reach or overcome the Si/SiO<sub>2</sub> potential barrier and become trapped into gate-oxide region. So we kept this in mind and re-designed our device which helps to get better HCI performance and device can pass HCI life time reliability test.

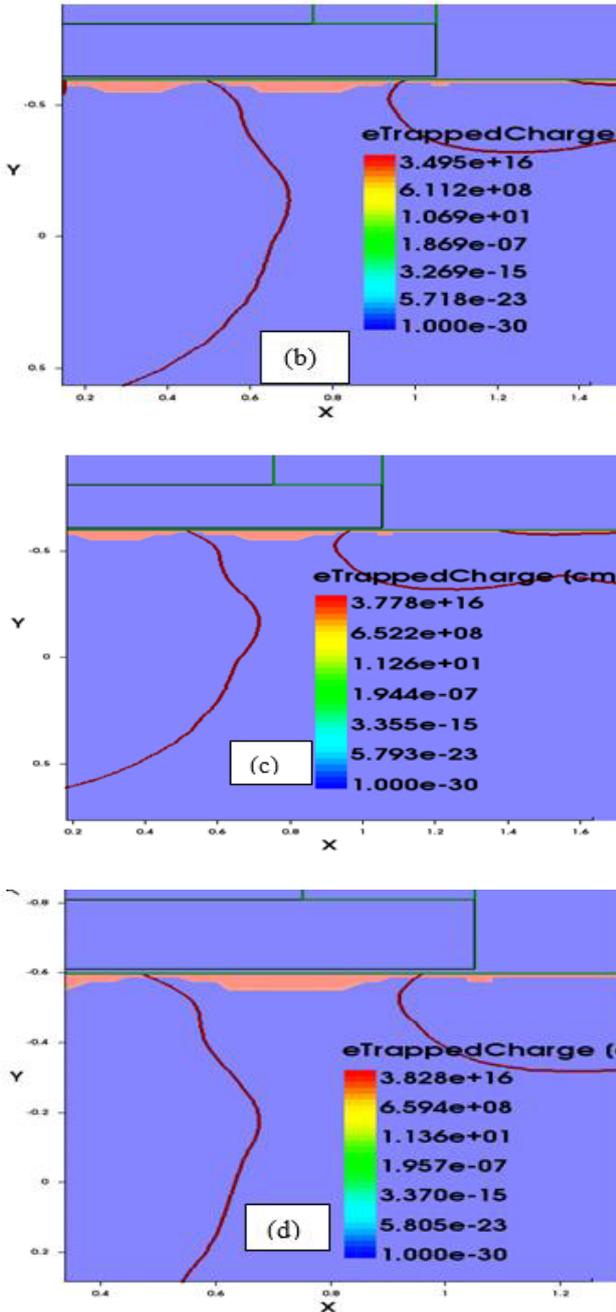


**Figure 1.** (a) Simulated structure of new proposed 60V nldmos and (b) Off-state bvd curves for proposed nldmos with different tilt angles (latid technique).



**Figure 2.** Flowchart of the experimental design





**Figure 3.** etrapped charge distribution for proposed n-lDMOS with various latid angles after 10,000 seconds of hci stress; (a) etrapped charge comparison between 30<sup>0</sup> and 7<sup>0</sup> angle (b) etrapped charge for 30<sup>0</sup> angle (c) etrapped charge for 45<sup>0</sup> angle and (d) etrapped charge for 60<sup>0</sup> angle.

Additionally it can see clearly or can be referred from figure 5, our proposed new nLDMOS structure shows better HCI performance compared to silicon HCI results as  $\Delta Ron\%$  and  $\Delta Id,sat\%$  curves of proposed structure are more flat compared to silicon data of reference structure and further from figure 5, one can notice that  $\Delta Ron\%$  is more severe than  $\Delta Idsat\%$  when compared between proposed and referred structures. So that shows less trap-charges are going into oxide that is gate-oxide and it is because impact ionization rate at offstate bvd is less than

referred structure as silicon data. It indicates our device design is good for ensuring long term reliability.

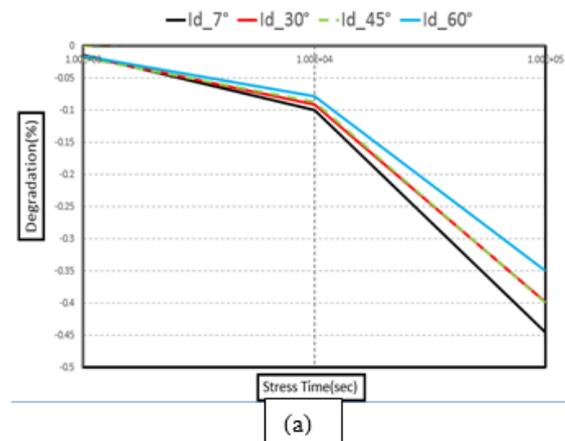
**Table 1.** Summary of eTrapped charge distribution and hci results of proposed n-lDMOS structure for different latid techniques.

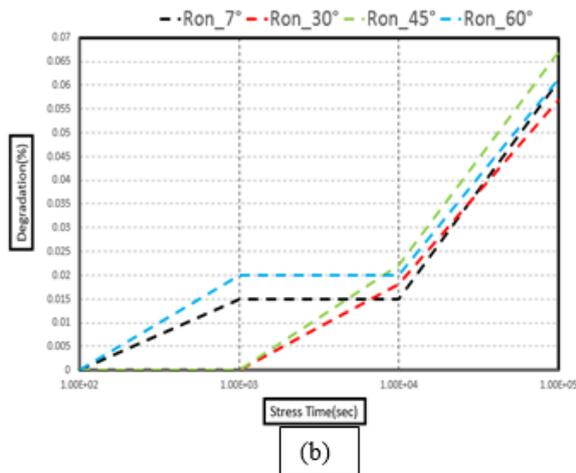
		Stress=0 sec	Stress=1e3 sec	Stress=1e4 sec	Stress=1e5 sec
eTrapped Charge (cm-3)	7°	2.078e*16	2.236e*16	3.495e*16	7.459e*16
	30°	2.078e*16	2.276e*16	3.495e*16	7.473e*16
	45°	2.078e*16	2.328e*16	3.778e*16	9.005e*16
	60°	2.078e*16	2.338e*16	3.828e*16	9.15e*16
Ron shift	7°	-	0.015%	0.015%	0.061%
	30°	-	0%	0.018%	0.054%
	45°	-	0%	0.022%	0.067%
	60°	-	0.02%	0.02%	0.062%
Idsat shift (degradation)	7°	-	-0.013%	-0.1%	-0.446%
	30°	-	-0.015%	-0.092%	-0.398%
	45°	-	-0.0175%	-0.087%	-0.4%
	60°	-	-0.016%	-0.078%	-0.35%

**Table 2.** Comparison of HCI results between proposed nLDMOS structure and reference silicon results.

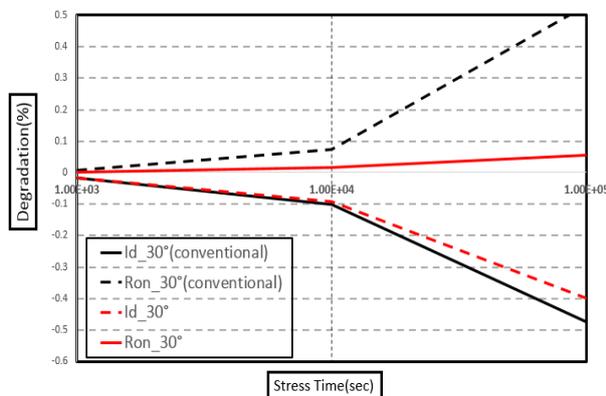
Stress time(s)	Silicon HCI results for 40V nLDMOS device (reference)		HCI results for our proposed nLDMOS structure	
	$\Delta Ron$	$\Delta Id,sat$	$\Delta Ron$	$\Delta Id,sat$
1e3	0.1%	0.09%	0~0.02%	0.013~0.017%
1e4	0.75%	0.5%	0.015~0.022%	0.077~0.1%

And we provided silicon HCI results for reference 40V nLDMOS device and to analyse clearly we put comparison table between HCI results of our new device structure and silicon HCI results of reference structure in Table 2. It can be easily understood that HCI performance of our proposed nLDMOS structure is very good as compared to silicon HCI results.





**Figure 4.** Plot of percentage HCI degradation Vs stress time for different latid (a) Plot of drain-current saturation ( $\Delta I_{d,sat}$ ) degradation Vs stress time and (b) Plot of on-resistance ( $\Delta R_{on}$ ) degradation Vs stress time.



**Figure 5.** Comparison of  $R_{on}(\%)$  and  $I_{d,sat}(\%)$  degradation between silicon data of reference nLDMOS and proposed nLDMOS structure

### 3.1 Conclusion

We have studied HCI performance in related to trapped charges at Si/SiO<sub>2</sub> interface and that can be optimized by implementing LATID technique for p-body. We also observe that in our proposed n-LDMOS device and may be possible for any nLDMOS devices, the 30° tilt angle implantation for p-body shows less traps thereby achieving better HCI results. Therefore the device life time reliability is improved. Hence it's one of the better solution for the devices to be optimized in such a way that impact-ionization hotspot at off-state  $b_{vd}$  should be away from gate and below the silicon interface and this type of device design helps to achieve less trap-charges and therefore improve HCI performance.

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